

VORAGO VA108x0 Schematic Symbol and PCB footprint

September 19, 2018 Version 2.0

VA10800/VA10820

Abstract

The VA108x0 comes in two packages, 128 plastic QFP and 128 ceramic QFP. This application note briefly describes how to use the associated va108xx.lbr file to create schematic symbols and PCB footprints in several PCB design tools such as Altium, OrCAD or PADS.

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1 Overview of library contents

Each PCB design tool vendor creates device, package and symbol libraries in their own formats. Each vendor has their own way of importing symbols from other vendors. EAGLE from Autodesk and Altium is one of the most popular PCB design tools. VORAGO provides the VA108x0 symbol and footprint in an EAGLE library. Customers can use the import function of the tool they subscribe to quickly create both the schematic part symbol and the PCB pad layout.

2 Eagle Footprint and Symbol

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The library (va108xx.lbr) consists of devices, symbols and footprints as shown in Figure 1. Four devices are offered; each package, ceramic and plastic, have two symbol options. See Figure 2. The “_split” option shows the device with pins grouped functionally. For example, power and grounds are shown in a separate block while the port pins are listed sequentially. The non-split option lists the pins in order of the mechanical package. Different designers prefer to use one or the other of these formats.

The plastic QFP has two layout options. One is for the part and the second is for a socket. See Figure 3.

Figure 1- Screen capture of the EAGLE library Table of Contents

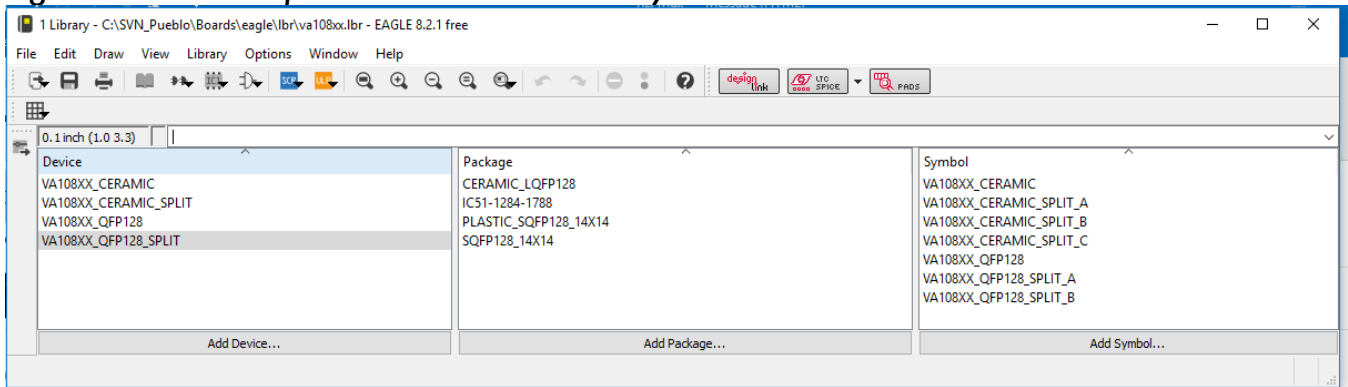
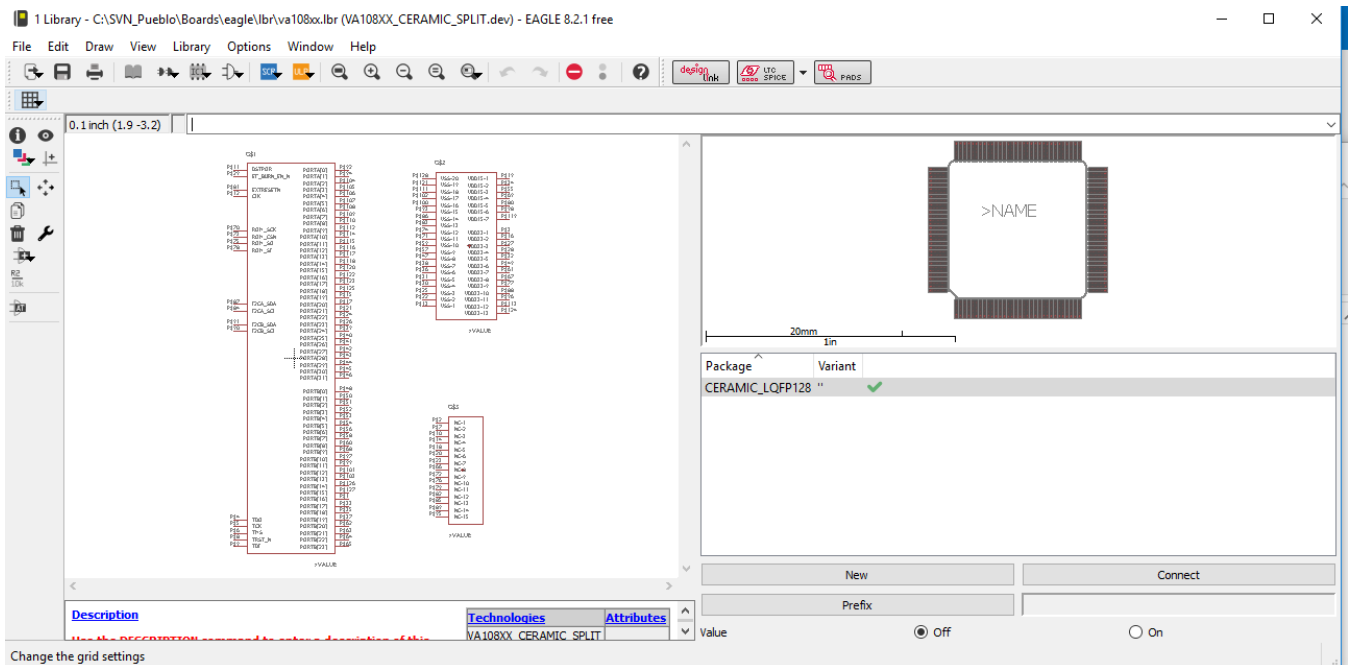
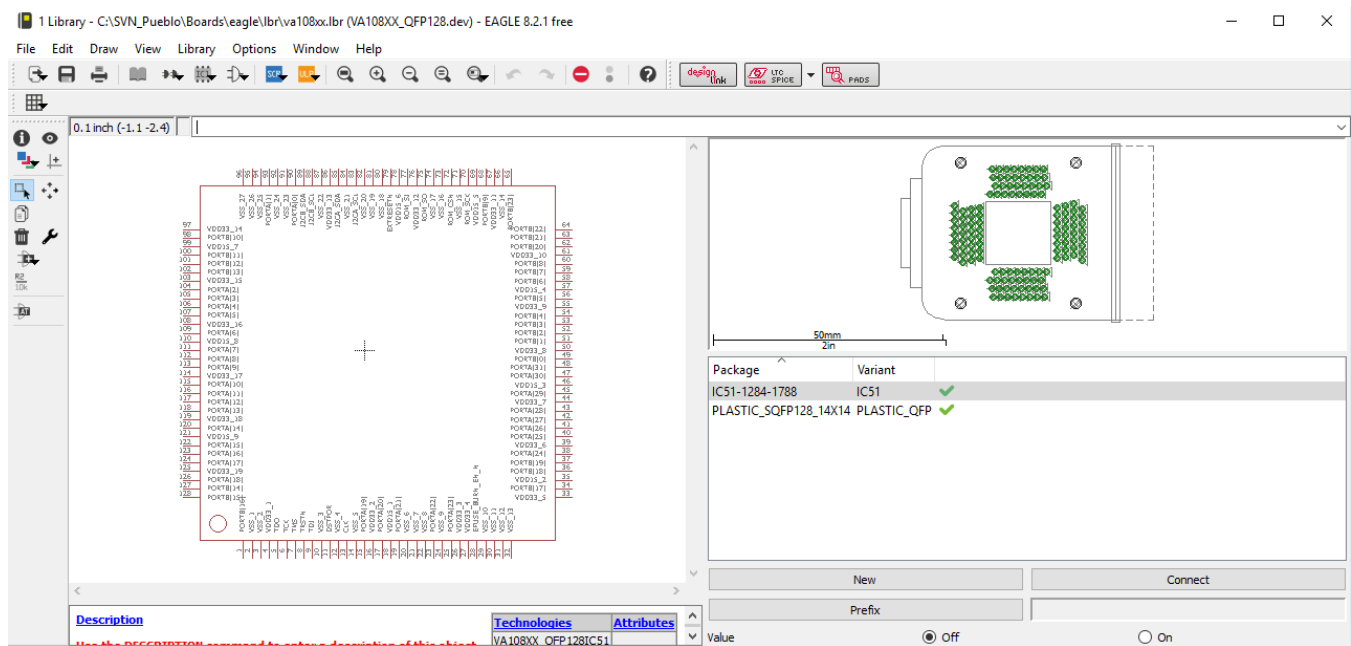


Figure 2 - “_split” symbol option showing pins grouped by functionality.



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Figure 3 - Plastic 128 QFP with socket layout



3 Altium Footprints and Symbols

The Altium component library is divided into two files: 1) va108xx.PcbLib, which contains the PCB footprint and 3D modeling, and 2) va108xx.SchLib which contains the schematic layout and pin associations. The easiest way to quickly view the footprint or component schematic is: File -> Open -> "filename".

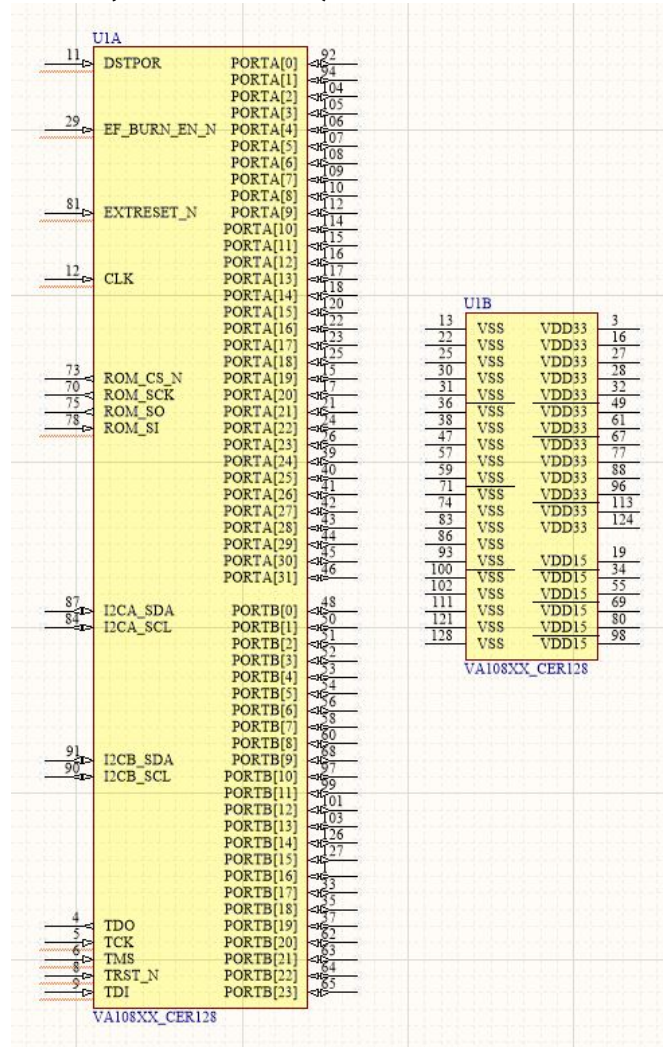
Three graphical schematics are provided based on your application preference. Each of the three models has both a Normal and Alternate1 graphical display mode. It is possible to view between display modes without impacting the connections.

3.1 VA108XX_CER128 symbol

This symbol option contains two parts, a large symbol for all signal pins and a second part grouping the power pins, with divider lines showing where sides change. The Alt1 view combines all the power pins into one grouped pin for VDD33, VDD15, and VSS for a simpler view. One schematic connection establishes nets on all physical of that type.

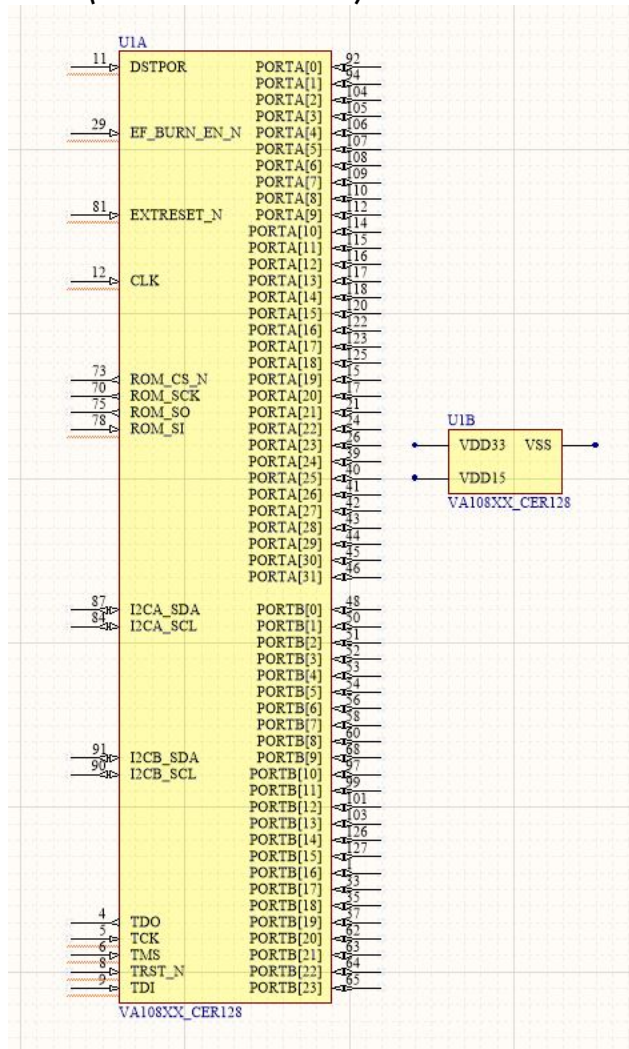
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Figure 4 - VA108XX_CER128 (Normal mode)



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Figure 5 - VA108XX_CER128 (Alternate 1 mode)



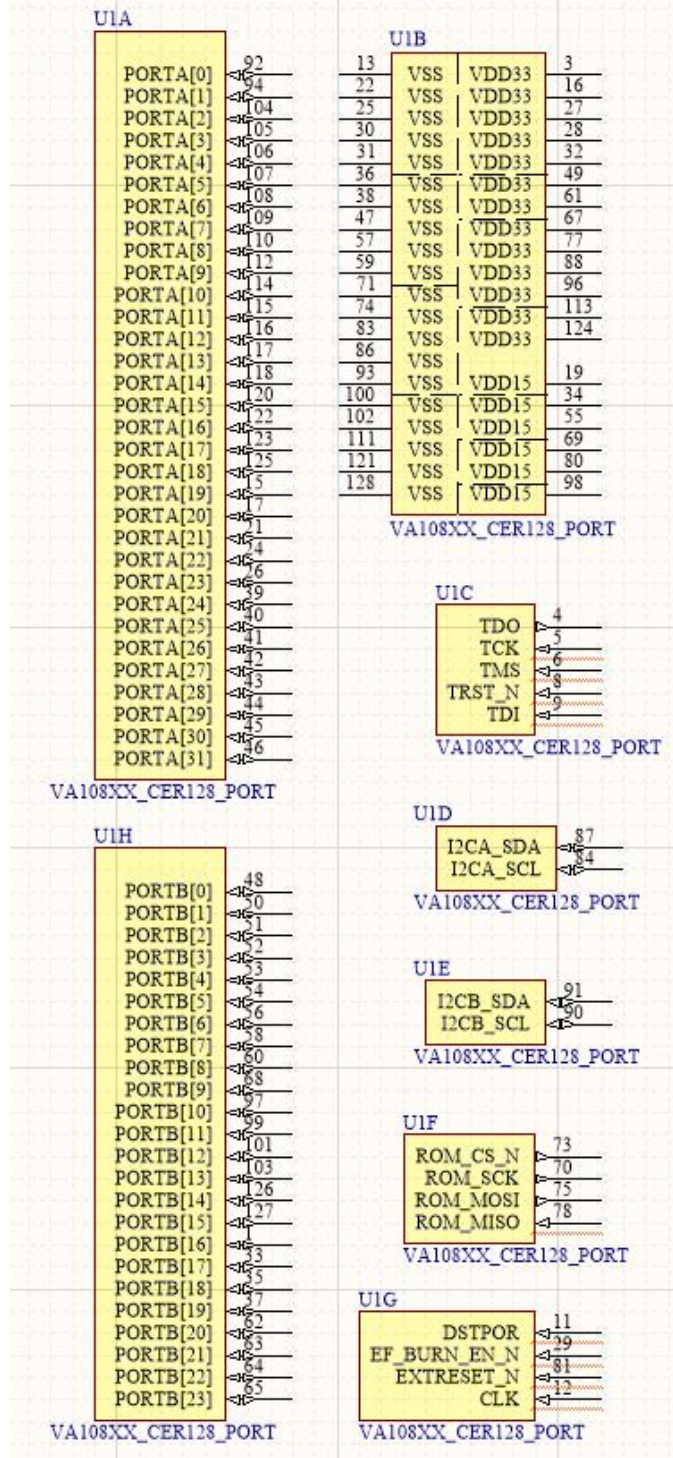
3.2 VA108XX_CER128_PORTS symbol

This symbol separates the chip into 8 parts: PortA, PortB, JTAG, I2CA, I2CB, boot ROM interface, system pins, and power as discrete pins grouped by side.

The "Alt1" representation expands the graphical symbol to show what functions are available for each port pin. Changing between the Normal/Alt1 view will not affect connections on the schematic.

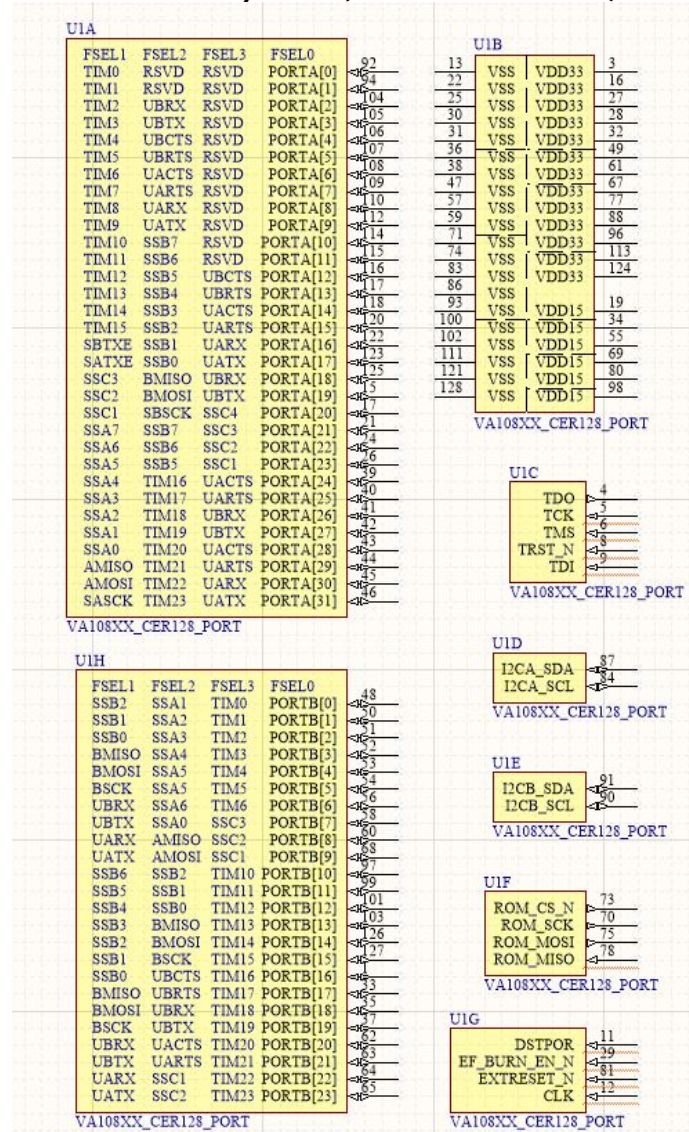
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Figure 6 - VA108XX_CER128_Port schematic symbol – (Normal Mode)



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Figure 7 – VA108XX_CER128_Ports Symbol (Alternate 1 mode)



3.3 VA108XX_CER128_SIDE symbol

This symbol is separated into 4 parts, one for each physical side of the va108xx. The "Alt1" representation expands the graphical symbol to show what functions are available for each port pin. Changing between the Normal/Alt1 view will not affect connections on the schematic.

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Figure 8 - VA108XX_CER128_SIDE symbol (Normal mode)

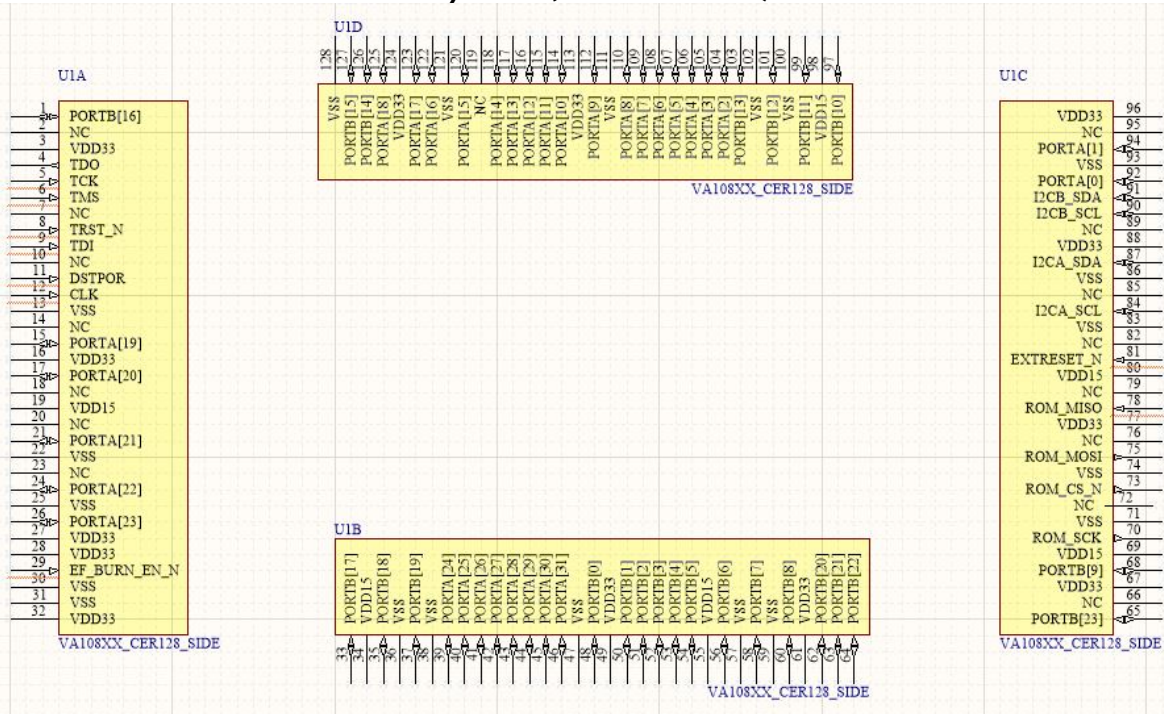


Figure 9 VA108XX_CER128_Side symbol (Alternate 1 mode)

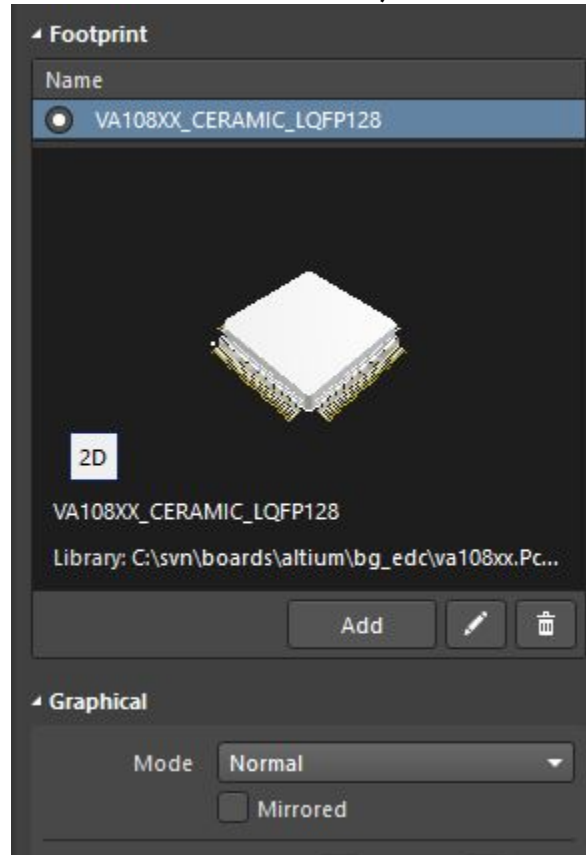


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3.4 Footprint and 3D model

PCB footprint along with 2D and 3D images are located in the va108xx.pcb.lib file. Either update the library search path to include this file or move the file to a location in the existing search path.

Figure 10 - VA108xx_Ceramic_LQFP128 model (click on the 2D button to toggle between 2D and 3D)



4 Conversion instructions

4.1 Cadence OrCAD specific

Please see <http://www.orcad.com/products/orcad-pcb-designer/overview> for latest import capabilities of OrCAD.

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4.2 PADS specific (Mentor Graphics)

Pulled from <https://www.pads.com>

With the latest version of PADS (VX.1) xDX designer has an Eagle schematic importer. It's as easy as file import Eagle, run the translator once to generate the properties to convert and then run the translator again with the correct property mappings.

Eagle files from version 6.5+ are supported

5 Alternate Function Assignment spreadsheet

The VA108x0 has port pins with 3 alternate functions such as UART, SPI or Timer pins. When defining which pins to use, it is useful to have a tool to help coordinate those assignments. A spreadsheet is provided with AN1213.zip file. The spreadsheet has columns for package pin number, side of the page (East, West, North, South), and the alternate functions. A system designer can use this sheet to make assignments based on availability of a function and its relative proximity to other ICs.

This sheet can also be used to add the other ICs on the PCB. It will function as a netlist for the ICs and can be compared against the PCB design tool.

VA108xx Pin Selection Help sheet													
Notes:													
1	Each port pin has 3 alternate functions that can be selected via software. The default value for each pin is Function Select 0 = General purpose input.												
2	Recommendation is to identify which timers and serial ports are needed in application, then select port pins with that function.												
3	Supplemental information can be inserted for connections to other ICs. This would essentially be the netlist of the design in a spreadsheet.												
MCU #1													
Plastic	Side of package	Ceramic		Pin/Function- 0	Function-1	Function-2	Function-3	JTAG#1	SPI boot device	Clock src			
128 pin #		128 pin #						10-pin	IC #1	IC #2	IC #3	IC #4	IC #5
48	East	46	East	PORTA[31]	SPI_SCKA	RTC[23]	UARTA_TX						
47	East	45	East	PORTA[30]	SPI_MOSIA	RTC[22]	UARTA_RX						
45	East	44	East	PORTA[29]	SPI_MISOA	RTC[21]	UARTA_RTSn						
43	East	43	East	PORTA[28]	SPI_SSELAn[0]	RTC[20]	UARTA_CTSn						
42	East	42	East	PORTA[27]	SPI_SSELAn[1]	RTC[19]	UARTB_TX						
41	East	41	East	PORTA[26]	SPI_SSELAn[2]	RTC[18]	UARTB_RX						
40	East	40	East	PORTA[25]	SPI_SSELAn[3]	RTC[17]	UARTB_RTSn						
38	East	39	East	PORTA[24]	SPI_SSELAn[4]	RTC[16]	UARTB_CTSn						
25	South	26	South	PORTA[23]	SPI_SSELAn[5]	SPI_SSELBn[5]	SPI_SSELCn[1]						
23	South	24	South	PORTA[22]	SPI_SSELAn[6]	SPI_SSELBn[6]	SPI_SSELCn[2]						
19	South	21	South	PORTA[21]	SPI_SSELAn[7]	SPI_SSELBn[7]	SPI_SSELCn[3]						
17	South	17	South	PORTA[20]	SPI_SSELCn[1]	SPI_SCKB	SPI_SSELCn[4]						
15	South	15	South	PORTA[19]	SPI_SSELCn[2]	SPI_MOSIB	UARTB_TX						
126	West	125	West	PORTA[18]	SPI_SSELCn[3]	SPI_MISOB	UARTB_RX						

6 Conclusions

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VORAGO is supplying CAD library files to enable users to quickly start their PCB design. Symbol and footprint models in native EAGLE and Altium tools are provided. Several versions of the symbol are provided to meet preferences of different customers. A separate spreadsheet is provided to assist engineers select which pins to place UART, SPI and Timer functions.

7 Other Resources

VORAGO VA10800 datasheet:

http://www.voragotech.com/sites/default/files/files/datasheets/VA10800_DS_0.pdf

VORAGO VA10820 datasheet:

http://www.voragotech.com/sites/default/files/files/datasheets/VA10820_DS_0.pdf

VORAGO MCU products: <http://www.voragotech.com/VORAGO-products>

VORAGO Application notes: <http://www.voragotech.com/resources>

VORAGO VA108xx REB1 board user guide: Part of Board Support Package (BSP)

<http://www.voragotech.com/products/reb1>

Altium Eagle converter instructions - <http://www.altium.com/video-eagle-importer>

Altium website - <http://www.altium.com>

Change Log

June 8, 2017 - Rev 1.0 Original release

Rev 2.0 September 15, 2018

- Added Altium component information

- Added Function Select spreadsheet in section 5.

- Updated table of contents and revision #