

AN1219

Software Reuse Between VA10820 and VA41628

Application Note

Apr 20, 2022, Version 1.0

VA10820/VA41628

1. Abstract

This application note reviews the differences between VORAGO's VA10820 and VA41628 MCUs and details the steps needed to use software developed for the VA10820 on the VA41628.

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2. Summary

User VA10820 software must be modified to run on the VA41628. The basic changes to be made to software are summarized as the following steps:

1. VA416xx 'common' folder (MCU and HAL drivers) must be used instead of the VA108x0 common folder / drivers. This includes the MCU header file (va416xx.h), system files, startup files, and optionally, peripheral drivers. All code files must reference the updated headers, and some peripheral names have changed slightly (SPI0, SPI1 ... vs SPIA, SPIB, ...).
2. VA41628 clock initialization (CLOCKGEN) code must be called during MCU initialization.
3. Memory regions are in different addresses. Any hard coded memory addresses (such as the RTT buffer) will need to be adjusted.
4. SYSCONFIG registers have changed slightly in the VA41628 and code will need adjustment.
5. GPIO code and GPIO alternate function selections must be modified to account for pin reordering. Not all pins on the VA41628 can perform all the alternate functions available on the VA10820, so some hardware / board layout changes may be necessary.
6. Timer initialization may need to change due to differences in clocking on the VA10820 and the VA41628. Some timer functions on the VA10820 are not available on the VA41628 (for example, a timer interrupt causing a hardware reset without any software intervention). Some timers on the VA41628 run at 2x the speed of the others, all 24 timers run at the same speed on the VA10820.
7. The interrupts on the VA41628 Cortex-M4 MCU work a bit differently than on the VA10820, so code relating to the NVIC and interrupt handlers will need to be modified. The VA10820 uses 32 interrupts that map to peripheral interrupts using the IRQSEL peripheral, the VA41628 has 256 fixed function interrupts.
8. The VA41628 has a dedicated watchdog timer, the VA10820 uses one of the 24 general purpose counter/timers as a watchdog. The watchdog initialization and software reset will need to be modified.
9. Code can optionally be modified to take advantage of additional features available in the VA41628, such as the floating-point unit (FPU), bit-banding, DMA, additional RAM.

3. System Files and Build Settings

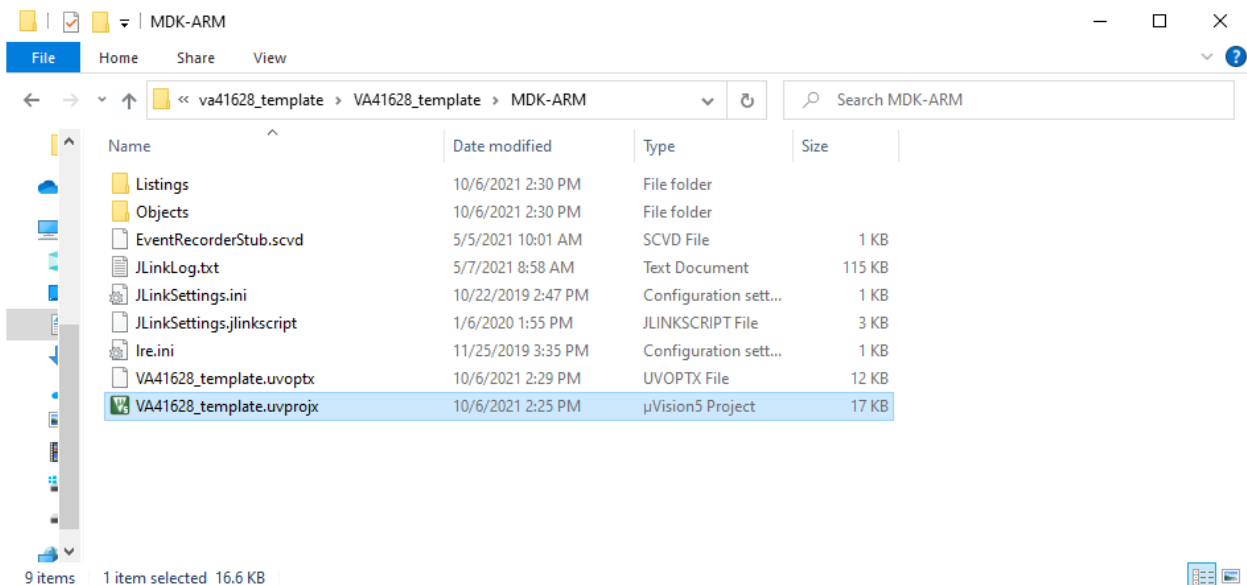
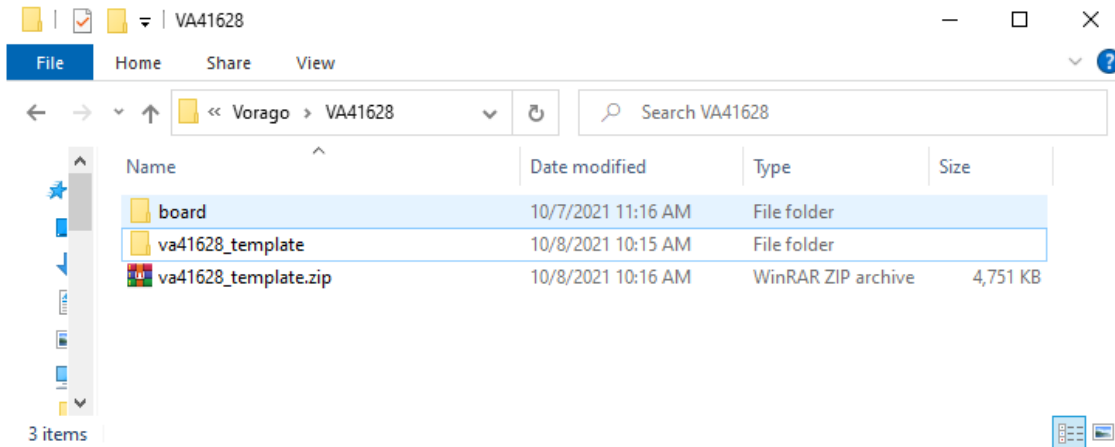
Make sure the VA416xx PACK file is installed. Double-click Vorago.VA416xx.1.0.5.pack to install. It is located in the /software/ folder of the EVK release package.

Projects being migrated from the VA10820 to the VA41628 must reference the 'common/mcu' folder of the VA41628 board support package, provided in the VA41628 EVK software. Some of the important system files to be replaced in your project are the following:

1. va108xx.h -> va416xx.h
2. system_va108xx.h -> system_va416xx.h
3. core_cm0.h -> core_cm4.h
4. system_va108xx.c -> system_va416xx.c

5. startup_va108xx.s -> startup_va416xx.s

The best way to ensure that these new system files are used is to start with a new template VA41628 project, provided with the EVK, and then move the user code into this new project. Extract va41628_template.zip (provided in the EVK package), then open the project.

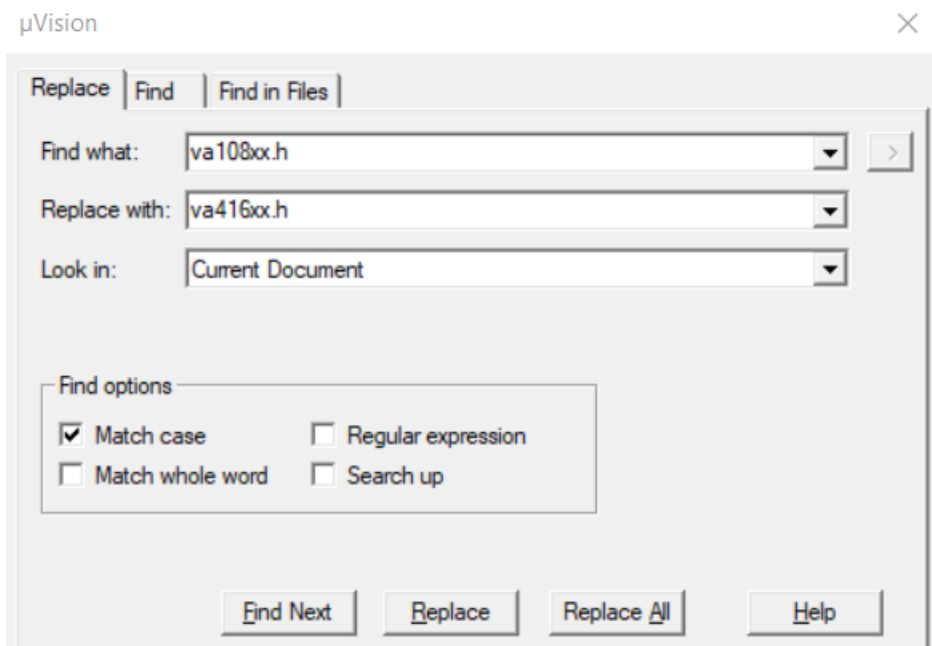


In this new project, add your existing source files, and add your main loop code to the existing main() function.

Open the source file 'board.h'. Set your external clock and/or XTAL value to match the clock rate on your board.

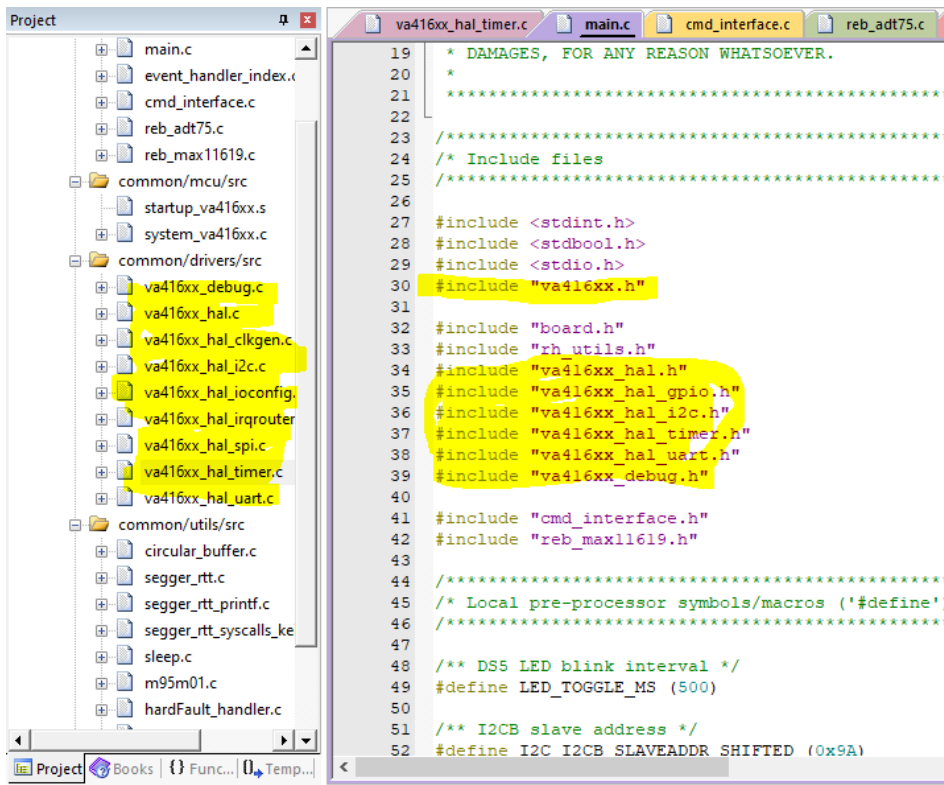
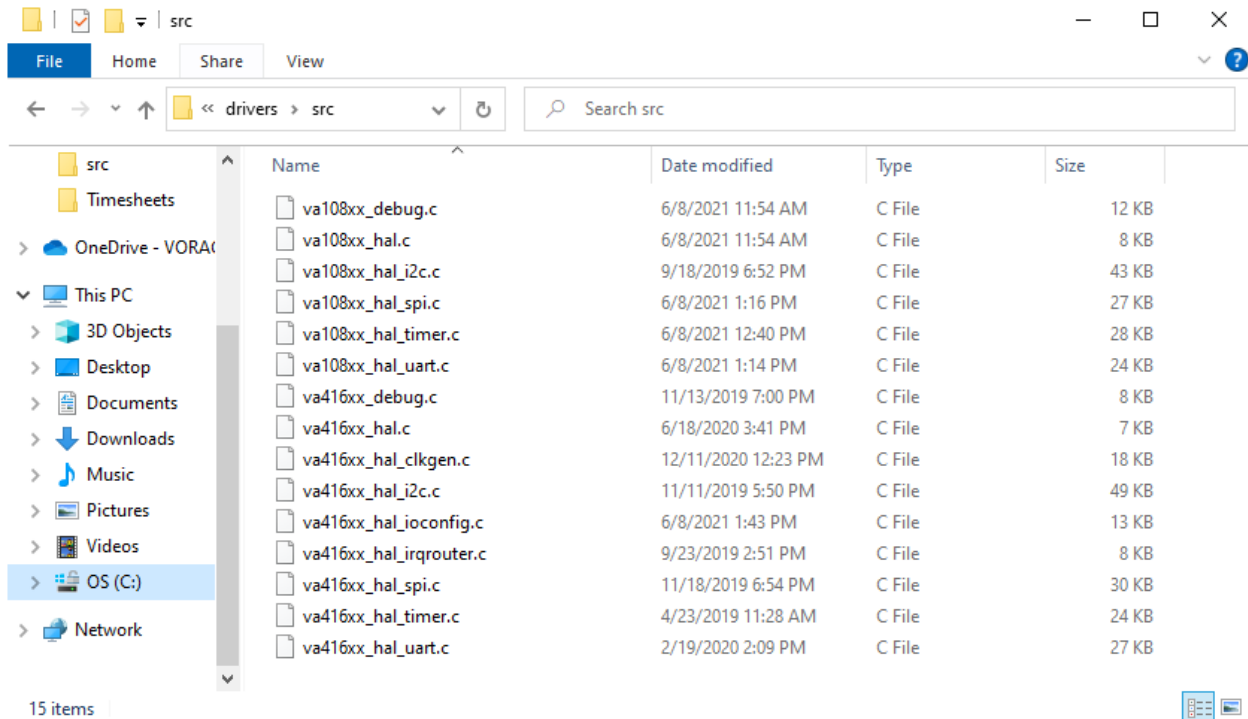
```
42
43 /** Hardware version (define for VA416x0 RevB) */
44 #define __MCU_HW_VER_REVB
45
46 /** Software Version */
47 #define SOFTWARE_VERSION_STR "2021_10_06_0v8"
48 #define SOFTWARE_VERSION (0x21100608) // 0.8
49
50 /* assert enable/disable (comment out to disable) */
51 //#define USE_ASSERT
52
53 /* enable watchdog (turn off if using breakpoints/debug) */
54 //#define ENABLE_WATCHDOG
55
56 /* Override external clocks (project specific) */
57 #undef EXTCLK
58 #undef XTAL
59 #undef HBO
60 #define EXTCLK (5000000UL) /* XTAL minus frequency */
61 #define XTAL (10000000UL) /* Oscillator frequency */
62 #define HBO (18500000UL) /* Internal HBO frequency (18-22mhz) */
63
64 /* Expected VREF voltage */
65 #define ADC_VREF (3.3f)
66
67 /* Internal in milliseconds between SysTick interrupts (defines how SysTick is init)*/
68 #define SYSTICK_INTERVAL_MS (1)
69
```

In existing source files from the VA10820 project, Replace all occurrences of 'va108xx.h' in the user code with 'va416xx.h'



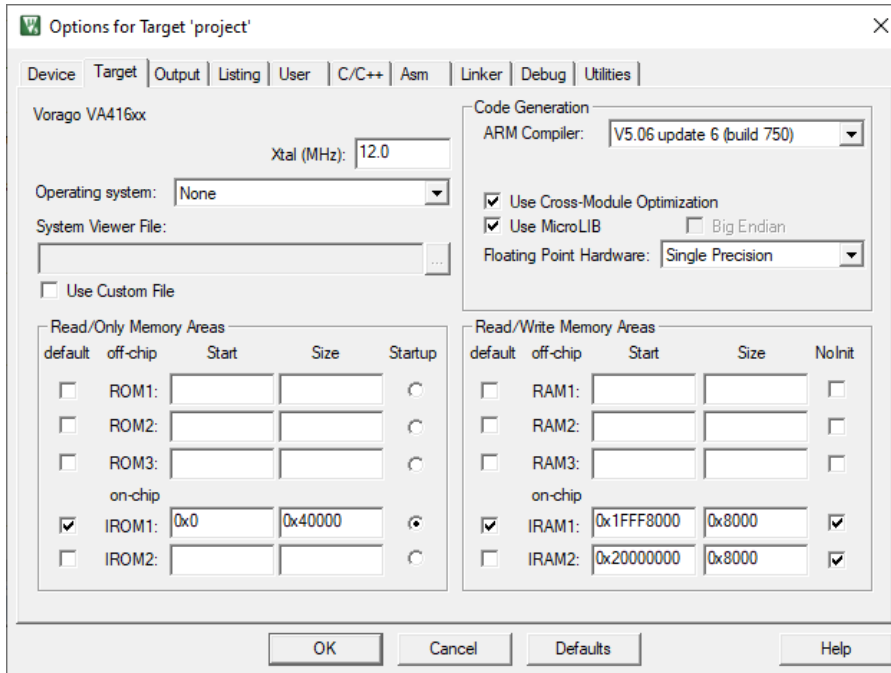
If using the VA108xx HAL in the project, add the VA416xx HAL files to /common/drivers/hdr/ and /common/drivers/src/. Include the VA416xx_hal files in the project and remove the VA108xx_hal files

from the project. In all project files, replace all #includes that reference va108xx_hal header files with va416xx_hal headers.



4. Memory Regions

Ensure the project settings under 'target' for your VA41628 project looks like the following:



If your project uses hard coded memory addresses, change these to fit within the ranges for IRAM1 or IRAM2 (0x1fff8000-0x2007FFFF).

5. GPIO Alternative Functions

5.1. VA10820 GPIO Function Select (FUNSEL)

Port pin default function	Alternative function 1 FUNSEL[1:0]=01	Alternative function 2 FUNSEL[1:0]=10	Alternative function 3 FUNSEL[1:0]=11
PORTA[31]	SPI_SCKA	TIM[23]	UARTA_TX
PORTA[30]	SPI_MOSIA	TIM[22]	UARTA_RX
PORTA[29]	SPI_MISOA	TIM[21]	UARTA_RTSn
PORTA[28]	SPI_SSELAN[0]	TIM[20]	UARTA_CTSn
PORTA[27]	SPI_SSELAN[1]	TIM[19]	UARTB_TX
PORTA[26]	SPI_SSELAN[2]	TIM[18]	UARTB_RX
PORTA[25]	SPI_SSELAN[3]	TIM[17]	UARTB_RTSn
PORTA[24]	SPI_SSELAN[4]	TIM[16]	UARTB_CTSn
PORTA[23]	SPI_SSELAN[5]	SPI_SSELBn[5]	SPI_SSELCn[1]
PORTA[22]	SPI_SSELAN[6]	SPI_SSELBn[6]	SPI_SSELCn[2]
PORTA[21]	SPI_SSELAN[7]	SPI_SSELBn[7]	SPI_SSELCn[3]
PORTA[20]	SPI_SSELCn[1]	SPI_SCKB	SPI_SSELCn[4]
PORTA[19]	SPI_SSELCn[2]	SPI_MOSIB	UARTB_TX
PORTA[18]	SPI_SSELCn[3]	SPI_MISOB	UARTB_RX
PORTA[17]	SPI_TXEMPTYA	SPI_SSELBn[0]	UARTA_TX

Port pin default function	Alternative function 1 FUNSEL[1:0]=01	Alternative function 2 FUNSEL[1:0]=10	Alternative function 3 FUNSEL[1:0]=11
PORTA[16]	SPI_TXEMPTYB	SPI_SSELBn[1]	UARTA_RX
PORTA[15]	TIM[15]	SPI_SSELBn[2]	UARTA_RTSn
PORTA[14]	TIM[14]	SPI_SSELBn[3]	UARTA_CTSn
PORTA[13]	TIM[13]	SPI_SSELBn[4]	UARTB_RTSn
PORTA[12]	TIM[12]	SPI_SSELBn[5]	UARTB_CTSn
PORTA[11]	TIM[11]	SPI_SSELBn[6]	LOCKUP (Out)
PORTA[10]	TIM[10]	SPI_SSELBn[7]	SYSRESETREQ (Out)
PORTA[9]	TIM[9]	UARTA_TX	SLEEPING (Out)
PORTA[8]	TIM[8]	UARTA_RX	HALTED (Out)
PORTA[7]	TIM[7]	UARTA_RTSn	TXEV (Out)
PORTA[6]	TIM[6]	UARTA_CTSn	RXEV (In)
PORTA[5]	TIM[5]	UARTB_RTSn	EDBGRQ (In)
PORTA[4]	TIM[4]	UARTB_CTSn	Unused
PORTA[3]	TIM[3]	UARTB_TX	I2CB_SCL
PORTA[2]	TIM[2]	UARTB_RX	I2CB_SDA
PORTA[1]	TIM[1]	I2CA_SCL	DBGRESTARTED (Out)
PORTA[0]	TIM[0]	I2CA_SDA	DBGRESTART (In)
PORTA[31]	SPI_SCKA	TIM[23]	UARTA_TX
PORTA[30]	SPI_MOSIA	TIM[22]	UARTA_RX
PORTB[23]	UARTA_TX	SPI_SSELCn[2]	TIM[23]
PORTB[22]	UARTA_RX	SPI_SSELCn[1]	TIM[22]
PORTB[21]	UARTB_TX	UARTA_RTSn	TIM[21]
PORTB[20]	UARTB_RX	UARTA_CTSn	TIM[20]
PORTB[19]	SPI_SCKB	UARTB_TX	TIM[19]
PORTB[18]	SPI_MOSIB	UARTB_RX	TIM[18]
PORTB[17]	SPI_MISOB	UARTB_RTSn	TIM[17]
PORTB[16]	SPI_SSELBn[0]	UARTB_CTSn	TIM[16]
PORTB[15]	SPI_SSELBn[1]	SPI_SCKB	TIM[15]
PORTB[14]	SPI_SSELBn[2]	SPI_MOSIB	TIM[14]
PORTB[13]	SPI_SSELBn[3]	SPI_MISOB	TIM[13]
PORTB[12]	SPI_SSELBn[4]	SPI_SSELBn[0]	TIM[12]
PORTB[11]	SPI_SSELBn[5]	SPI_SSELBn[1]	TIM[11]
PORTB[10]	SPI_SSELBn[6]	SPI_SSELBn[2]	TIM[10]
PORTB[9]	UARTA_TX	SPI_SCKA	SPI_SSELCn[1]
PORTB[8]	UARTA_RX	SPI_MOSIA	SPI_SSELCn[2]
PORTB[7]	UARTB_TX	SPI_MISOA	SPI_SSELCn[3]
PORTB[6]	UARTB_RX	SPI_SSELAN[0]	TIM[6]
PORTB[5]	SPI_SCKB	SPI_SSELAN[6]	TIM[5]
PORTB[4]	SPI_MOSIB	SPI_SSELAN[5]	TIM[4]

Port pin default function	Alternative function 1 FUNSEL[1:0]=01	Alternative function 2 FUNSEL[1:0]=10	Alternative function 3 FUNSEL[1:0]=11
PORTB[3]	SPI_MISOB	SPI_SSELAN[4]	TIM[3]
PORTB[2]	SPI_SSELBn[0]	SPI_SSELAN[3]	TIM[2]
PORTB[1]	SPI_SSELBn[1]	SPI_SSELAN[2]	TIM[1]
PORTB[0]	SPI_SSELBn[2]	SPI_SSELAN[1]	TIM[0]

5.2. VA41628 GPIO Function Select (FUNSEL)

Port pin default function	Alternative function 1 FUNSEL[1:0]=01	Alternative function 2 FUNSEL[1:0]=10	Alternative function 3 FUNSEL[1:0]=11
PORTA[0]	TIM[0]	SPI2_SSn4	UART0_RTSn
PORTA[1]	TIM[1]	SPI2_SSn3	UART0_CTSn
PORTA[2]	TIM[2]	SPI2_SSn2	UART0_TX
PORTA[3]	TIM[3]	SPI2_SSn1	UART0_RX
PORTA[4]	TIM[4]	SPI2_SSn0	Not assigned
PORTA[5]	TIM[5]	SPI2_SCK	Not assigned
PORTA[6]	TIM[6]	SPI2_MISO	Not assigned
PORTA[7]	TIM[7]	SPI2_MOSI	Not assigned
PORTA[8]	Not assigned	SPI2_SSn6	TIM[8]
PORTA[9]	Not assigned	SPI2_SSn5	Not assigned
PORTA[10]	Not assigned	TIM[23]	Not assigned
PORTA[11]	Not assigned	TIM[22]	Not assigned
PORTA[12]	Not assigned	TIM[21]	Not assigned
PORTA[13]	Not assigned	TIM[20]	Not assigned
PORTA[14]	Not assigned	TIM[19]	Not assigned
PORTA[15]	Not assigned	TIM[18]	Not assigned
PORTB[0]	Not assigned	TIM[17]	SPI1_SSn7
PORTB[1]	Not assigned	TIM[16]	SPI1_SSn6
PORTB[2]	Not assigned	TIM[15]	SPI1_SSn5
PORTB[3]	Not assigned	TIM[14]	SPI1_SSn4
PORTB[4]	Not assigned	TIM[13]	SPI1_SSn3
PORTB[12]	SPI0_SSn2	TIM[5]	UART1_RTSn
PORTB[13]	SPI0_SSn1	TIM[4]	UART1_CTSn
PORTB[14]	SPI0_SSn0	TIM[3]	UART1_TX
PORTB[15]	SPI0_SCK	TIM[2]	UART1_RX
PORTC[0]	SPI0_MISO	TIM[1]	Not assigned
PORTC[1]	SPI0_MOSI	TIM[0]	Not assigned
PORTC[2]	Not assigned	UART0_RTSn	Not assigned
PORTC[3]	Not assigned	UART0_CTSn	Not assigned
PORTC[4]	Not assigned	UART0_TX	Not assigned
PORTC[5]	Not assigned	UART0_RX	Not assigned
PORTC[6]	Not assigned	Not assigned	Not assigned
PORTC[7]	Not assigned	SPI1_SSn1	Not assigned
PORTC[8]	Not assigned	SPI1_SSn0	Not assigned
PORTC[9]	Not assigned	SPI1_SCK	Not assigned
PORTC[10]	Not assigned	SPI1_MISO	Not assigned
PORTC[11]	Not assigned	SPI1_MOSI	Not assigned
PORTC[12]	Not assigned	Not assigned	Not assigned

Port pin default function	Alternative function 1 FUNSEL[1:0]=01	Alternative function 2 FUNSEL[1:0]=10	Alternative function 3 FUNSEL[1:0]=11
PORTC[14]	Not assigned	UART2_TX	Not assigned
PORTD[10]	Not assigned	TIM[10]	UART1_CTSn
PORTD[11]	Not assigned	TIM[11]	UART1_TX
PORTD[12]	Not assigned	TIM[12]	UART1_RX
PORTD[13]	Not assigned	TIM[13]	Not assigned
PORTD[14]	Not assigned	TIM[14]	Not assigned
PORTD[15]	Not assigned	TIM[15]	Not assigned
PORTE[0]	Not assigned	TIM[16]	UART0_RTSn
PORTE[1]	Not assigned	TIM[17]	UART0_CTSn
PORTE[2]	Not assigned	TIM[18]	UART0_TX
PORTE[3]	Not assigned	TIM[19]	UART0_RX
PORTE[4]	Not assigned	TIM[20]	Not assigned
PORTE[5]	Not assigned	TIM[21]	SPI1_SSn7
PORTE[6]	Not assigned	TIM[22]	SPI1_SSn6
PORTE[7]	Not assigned	TIM[23]	SPI1_SSn5
PORTE[8]	Not assigned	SPI1_SSn4	TIM[16]
PORTE[9]	Not assigned	SPI1_SSn3	TIM[17]
PORTE[12]	Not assigned	SPI1_SSn0	TIM[20]
PORTE[13]	Not assigned	SPI1_SCK	TIM[21]
PORTE[14]	Not assigned	SPI1_MISO	TIM[22]
PORTE[15]	Not assigned	SPI1_MOSI	TIM[23]
PORTF[0]	Not assigned	SPI2_SSn4	TIM[0]
PORTF[1]	Not assigned	SPI2_SSn3	TIM[1]
PORTF[9]	UART2_RX	Not assigned	TIM[9]
PORTF[11]	UART1_CTSn	Not assigned	TIM[11]
PORTF[12]	UART1_TX	Not assigned	TIM[12]
PORTF[13]	UART1_RX	TIM[19]	Not assigned
PORTF[14]	UART0_RTSn	TIM[20]	Not assigned
PORTF[15]	UART0_CTSn	TIM[21]	Not assigned
PORTG[0]	UART0_TX	TIM[22]	Not assigned
PORTG[1]	UART0_RX	TIM[23]	Not assigned
PORTG[2]	TIM[9]	SPI1_SSn0	Not assigned
PORTG[3]	TIM[10]	SPI1_SCK	Not assigned
PORTG[4]	SPI1_SSn3	SPI1_MISO	Not assigned
PORTG[5]	SPI1_SSn2	Not assigned	Not assigned
PORTG[6]	SPI1_SSn1	TIM[12]	Not assigned
PORTG[7]	Not assigned	Not assigned	Not assigned

6. PERIPHERAL FUNCTION SELECT MAPPING TABLE

VA10820 UARTA corresponds to VA41628 UART0.

VA10820 UARTB corresponds to VA41628 UART1.

VA10820 SPIA corresponds to VA41628 SPI0.

VA10820 SPIA has 8 chip selects: SPI_SSELAN[7:0].

VA416xx SPI0 has 3 chip selects: SPI0_SSn2, SPI0_SSn1, SPI0_SSn0.

VA10820 SPIB corresponds to VA41628 SPI1.

VA10820 SPIB has 8 chip selects: SPI_SSELBn[7:0].

VA416xx SPI1 has 8 chip selects: SPI1_SSn7 through SPI1_SSn0.

VA10820 SPIC corresponds to VA41628 SPI2.

VA10820 SPIC has 4 chip selects: SPI_SSELCn[4:1].

VA416xx SPI2 has 7 chip selects: SPI2_SSn6 through SPI2_SSn0.

VA10820 has only three SPI interfaces. VA41628 has four SPIs.

VA10820 SPIC shares its pins with the ROM SPI interface.

VA41628 SPI3 shares its pins with the ROM SPI interface.

VA10820 has only two I2C interfaces. VA41628 has three I2Cs.

VA10820 Port pin default function	VA10820 Special Functions	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO
PORTA[31]	SPI_SCKA	SPI0_SCK PORTB[15]			
	TIM[23]	TIM[23] PORTA[10]	TIM[23] PORTE[7]	TIM[23] PORTG[1]	
	UARTA_TX	UART0_TX PORTA[2]	UART0_TX PORTC[4]	UART0_TX PORTE[2]	UART0_TX PORTG[0]
PORTA[30]	SPI_MOSIA	SPI0_MOSI PORTC[1]			
	TIM[22]	TIM[22] PORTA[11]	TIM[22] PORTE[6]	TIM[22] PORTG[0]	
	UARTA_RX	UART0_RX PORTA[3]	UART0_RX PORTC[5]	UART0_RX PORTE[3]	UART0_RX PORTG[1]
PORTA[29]	SPI_MISOA	SPI0_MISO PORTC[0]			
	TIM[21]	TIM[21] PORTA[12]	TIM[21] PORTE[5]	TIM[21] PORTF[15]	
	UARTA_RTSn	UART0_RTSn PORTA[0]	UART0_RTSn PORTC[2]	UART0_RTSn PORTE[0]	UART0_RTSn PORTF[14]
PORTA[28]	SPI_SSELAN[0]	SPI0_SSn0 PORTB[14]			
	TIM[20]	TIM[20] PORTA[13]	TIM[20] PORTE[4]	TIM[20] PORTF[14]	
	UARTA_CTSn	UART0_CTSn PORTA[1]	UART0_CTSn PORTC[3]	UART0_CTSn PORTE[1]	UART0_CTSn PORTF[15]

VA10820 Port pin default function	VA10820 Special Functions	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO
PORTA[27]	SPI_SSELAN[1]	SPI0_SSn1 PORTB[13]			
	TIM[19]	TIM[19] PORTA[14]	TIM[19] PORTE[3]	TIM[19] PORTF[13]	
	UARTB_TX	UART1_TX PORTB[14]	UART1_TX PORTD[11]	UART1_TX PORTF[12]	
PORTA[26]	SPI_SSELAN[2]	SPI0_SSn2 PORTB[12]			
	TIM[18]	TIM[18] PORTA[15]	TIM[18] PORTE[2]		
	UARTB_RX	UART1_RX PORTB[15]	UART1_RX PORTD[12]	UART1_RX PORTF[13]	
PORTA[25]	SPI_SSELAN[3]	No equivalent SSn function on VA41628 SPI0 – SPI1 could be used			
	TIM[17]	TIM[17] PORTB[0]	TIM[17] PORTE[1]		
	UARTB_RTSn	UART1_RTSn PORTB[12]	UART1_RTSn PORTD[9]	UART1_RTSn PORTF[10]	
PORTA[24]	SPI_SSELAN[4]	No equivalent SSn function on VA41628 SPI0 – SPI1 could be used			
	TIM[16]	TIM[16] PORTB[1]	TIM[16] PORTE[0]	TIM[16] PORTE[8]	
	UARTB_CTSn	UART1_CTSn PORTB[13]	UART1_CTSn PORTD[10]	UART1_CTSn PORTF[11]	
PORTA[23]	SPI_SSELAN[5]	No equivalent SSn function on VA41628 SPI0 - SPI1 could be used			
	SPI_SSELBn[5]	SPI1_SSn5 PORTB[2]			
	SPI_SSELCn[1]	SPI2_SSn1 PORTA[3]			
PORTA[22]	SPI_SSELAN[6]	No equivalent SSn function on VA41628 SPI0 – SPI1 could be used			
	SPI_SSELBn[6]	SPI1_SSn6 PORTB[1]			
	SPI_SSELCn[2]	SPI2_SSn2 PORTA[2]			
PORTA[21]	SPI_SSELAN[7]	No equivalent SSn function on VA41628 SPI0 – SPI1 could be used			
	SPI_SSELBn[7]	SPI1_SSn7 PORTB[0]			
	SPI_SSELCn[3]	SPI2_SSn3 PORTA[1]			
PORTA[20]	SPI_SSELCn[1]	SPI2_SSn1 PORTA[3]			
	SPI_SCKB	SPI1_SCK PORTC[9]	SPI1_SCK PORTE[13]	SPI1_SCK PORTG[3]	
	SPI_SSELCn[4]	SPI2_SSn4 PORTA[0]			
PORTA[19]	SPI_SSELCn[2]	SPI2_SSn2 PORTA[2]			
	SPI_MOSIB	SPI1_MOSI PORTC[11]	SPI1_MOSI PORTE[15]		
	UARTB_TX	UART1_TX PORTB[14]	UART1_TX PORTD[11]	UART1_TX PORTF[12]	
PORTA[18]	SPI_SSELCn[3]	SPI2_SSn3 PORTA[1]			
	SPI_MISOB	SPI1_MISO PORTC[10]	SPI1_MISO PORTE[14]	SPI1_MISO PORTG[4]	

VA10820 Port pin default function	VA10820 Special Functions	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO
	UARTB_RX	UART1_RX PORTB[15]	UART1_RX PORTD[12]	UART1_RX PORTF[13]	
PORTA[17]	SPI_TXEMPTYA	No equivalent function on VA41628			
	SPI_SSELBn[0]	SPI1_SSn0 PORTC[8]	SPI1_SSn0 PORTE[12]	SPI1_SSn0 PORTG[2]	
	UARTA_TX	UART0_TX PORTA[2]	UART0_TX PORTC[4]	UART0_TX PORTE[2]	UART0_TX PORTG[0]
PORTA[16]	SPI_TXEMPTYB	No equivalent function on VA41628			
	SPI_SSELBn[1]	SPI1_SSn1 PORTC[7]	SPI1_SSn1 PORTG[6]		
	UARTA_RX	UART0_RX PORTA[3]	UART0_RX PORTC[5]	UART0_RX PORTE[3]	UART0_RX PORTG[1]
PORTA[15]	TIM[15]	TIM[15] PORTB[2]	TIM[15] PORTD[15]		
	SPI_SSELBn[2]	SPI1_SSn2 PORTG[5]			
	UARTA_RTSn	UART0_RTSn PORTA[0]	UART0_RTSn PORTC[2]	UART0_RTSn PORTE[0]	UART0_RTSn PORTF[14]
PORTA[14]	TIM[14]	TIM[14] PORTB[3]	TIM[14] PORTD[14]		
	SPI_SSELBn[3]	SPI1_SSn3 PORTB[4]	SPI1_SSn3 PORTE[9]	SPI1_SSn3 PORTG[4]	
	UARTA_CTSn	UART0_CTSn PORTA[1]	UART0_CTSn PORTC[3]	UART0_CTSn PORTE[1]	UART0_CTSn PORTF[15]
PORTA[13]	TIM[13]	TIM[13] PORTB[4]	TIM[13] PORTD[13]		
	SPI_SSELBn[4]	SPI_SSn4 PORTB[3]	SPI_SSn4 PORTE[8]		
	UARTB_RTSn	UART1_RTSn PORTB[12]	UART1_RTSn PORTD[9]	UART1_RTSn PORTF[10]	
PORTA[12]	TIM[12]	TIM[12] PORTD[12]	TIM[12] PORTF[12]	TIM[12] PORTG[6]	
	SPI_SSELBn[5]	SPI1_SSn5 PORTB[2]			
	UARTB_CTSn	UART1_CTSn PORTB[13]	UART1_CTSn PORTD[10]	UART1_CTSn PORTF[11]	
PORTA[11]	TIM[11]	TIM[11] PORTD[11]	TIM[11] PORTF[11]		
	SPI_SSELBn[6]	SPI1_SSn6 PORTB[1]			
	LOCKUP (Out)	No equivalent function on VA41628			
PORTA[10]	TIM[10]	TIM[10] PORTD[10]	TIM[10] PORTF[10]	TIM[10] PORTG[3]	
	SPI_SSELBn[7]	SPI1_SSn7 PORTB[0]			
	SYSRESETREQ (Out)	No equivalent function on VA41628			
PORTA[9]	TIM[9]	TIM[9] PORTD[9]	TIM[9] PORTG[2]		
	UARTA_TX	UART0_TX PORTA[2]	UART0_TX PORTC[4]	UART0_TX PORTE[2]	UART0_TX PORTG[0]
	SLEEPING (Out)	No equivalent function on VA41628			

VA10820 Port pin default function	VA10820 Special Functions	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO
PORTA[8]	TIM[8]	TIM[8] PORTA[8]			
	UARTA_RX	UART0_RX PORTA[3]	UART0_RX PORTC[5]	UART0_RX PORTE[3]	UART0_RX PORTG[1]
	HALTED (Out)	No equivalent function on VA41628			
PORTA[7]	TIM[7]	TIM[7] PORTA[7]			
	UARTA_RTSn	UART0_RTSn PORTA[0]	UART0_RTSn PORTC[2]	UART0_RTSn PORTE[0]	UART0_RTSn PORTF[14]
	TXEV (Out)	No equivalent function on VA41628			
PORTA[6]	TIM[6]	TIM[6] PORTA[6]			
	UARTA_CTSn	UART0_CTSn PORTA[1]	UART0_CTSn PORTC[3]	UART0_CTSn PORTE[1]	UART0_CTSn PORTF[15]
	RXEVI (In)	No equivalent function on VA41628			
PORTA[5]	TIM[5]	TIM[5] PORTA[5]	TIM[5] PORTB[12]		
	UARTB_RTSn	UART1_RTSn PORTB[12]	UART1_RTSn PORTD[9]	UART1_RTSn PORTF[10]	
	EDBGRQ (In)	No equivalent function on VA41628			
PORTA[4]	TIM[4]	TIM[4] PORTA[4]	TIM[4] PORTB[13]		
	UARTB_CTSn	UART1_CTSn PORTB[13]	UART1_CTSn PORTD[10]	UART1_CTSn PORTF[11]	
PORTA[3]	TIM[3]	TIM[3] PORTA[3]	TIM[3] PORTB[14]		
	UARTB_TX	UART1_TX PORTB[14]	UART1_TX PORTD[11]	UART1_TX PORTF[12]	
	I2CB_SCL	I2C not shared with GPIO on VA41628			
PORTA[2]	TIM[2]	TIM[2] PORTA[2]	TIM[2] PORTB[15]		
	UARTB_RX	UART1_RX PORTB[15]	UART1_RX PORTD[12]	UART1_RX PORTF[13]	
	I2CB_SDA	I2C not shared with GPIO on VA41628			
PORTA[1]	TIM[1]	TIM[1] PORTA[1]	TIM[1] PORTC[0]	TIM[1] PORTF[1]	
	I2CA_SCL	I2C not shared with GPIO on VA41628			
	DBGRESTARTED (Out) ²	No equivalent function on VA41628			
PORTA[0]	TIM[0]	TIM[0] PORTA[0]	TIM[0] PORTC[1]	TIM[0] PORTF[0]	
	I2CA_SDA	I2C not shared with GPIO on VA41628			
	DBGRESTART (In)	No equivalent function on VA41628			
PORTB[23]	UARTA_TX	UART0_TX PORTA[2]	UART0_TX PORTC[4]	UART0_TX PORTE[2]	UART0_TX PORTG[0]
	SPI_SSELCn[2]	SPI2_SS2 PORTA[2]			
	TIM[23]	TIM[23] PORTA[10]	TIM[23] PORTE[7]	TIM[23] PORTG[1]	

VA10820 Port pin default function	VA10820 Special Functions	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO
PORTB[22]	UARTA_RX	UART0_RX PORTA[3]	UART0_RX PORTC[5]	UART0_RX PORTE[3]	UART0_RX PORTG[1]
	SPI_SSELCn[1]	SPI2_SSn1 PORTA[3]			
	TIM[22]	TIM[22] PORTA[11]	TIM[22] PORTE[6]	TIM[22] PORTG[0]	
PORTB[21]	UARTB_TX	UART1_TX PORTB[14]	UART1_TX PORTD[11]	UART1_TX PORTF[12]	
	UARTA_RTSn	UART0_RTSn PORTA[0]	UART0_RTSn PORTC[2]	UART0_RTSn PORTE[0]	UART0_RTSn PORTF[14]
	TIM[21]	TIM[21] PORTA[12]	TIM[21] PORTE[5]	TIM[21] PORTF[15]	
PORTB[20]	UARTB_RX	UART1_RX PORTB[15]	UART1_RX PORTD[12]	UART1_RX PORTF[13]	
	UARTA_CTSn	UART0_CTSn PORTA[1]	UART0_CTSn PORTC[3]	UART0_CTSn PORTE[1]	UART0_CTSn PORTF[15]
	TIM[20]	TIM[20] PORTA[13]	TIM[20] PORTE[4]	TIM[20] PORTF[14]	
PORTB[19]	SPI_SCKB	SPI1_SCK PORTC[9]	SPI1_SCK PORTE[13]	SPI1_SCK PORTG[3]	
	UARTB_TX	UART1_TX PORTB[14]	UART1_TX PORTD[11]	UART1_TX PORTF[12]	
	TIM[19]	TIM[19] PORTA[14]	TIM[19] PORTE[3]	TIM[19] PORTF[13]	
PORTB[18]	SPI_MOSIB	SPI1_MOSI PORTC[11]	SPI1_MOSI PORTE[15]		
	UARTB_RX	UART1_RX PORTB[15]	UART1_RX PORTD[12]	UART1_RX PORTF[13]	
	TIM[18]	TIM[18] PORTA[15]	TIM[18] PORTE[2]		
PORTB[17]	SPI_MISOB	SPI1_MISO PORTC[10]	SPI1_MISO PORTE[14]	SPI1_MISO PORTG[4]	
	UARTB_RTSn	UART1_RTSn PORTB[12]	UART1_RTSn PORTD[9]	UART1_RTSn PORTF[10]	
	TIM[17]	TIM[17] PORTB[0]	TIM[17] PORTE[1]		
PORTB[16]	SPI_SSELBn[0]	SPI1_SSn0 PORTC[8]	SPI1_SSn0 PORTE[12]	SPI1_SSn0 PORTE[2]	
	UARTB_CTSn	UART1_CTSn PORTB[13]	UART1_CTSn PORTD[10]	UART1_CTSn PORTF[11]	
	TIM[16]	TIM[16] PORTB[1]	TIM[16] PORTE[0]	TIM[16] PORTE[8]	
PORTB[15]	SPI_SSELBn[1]	SPI1_SSn1 PORTC[7]	SPI1_SSn1 PORTG[6]		
	SPI_SCKB	SPI1_SCK PORTC[9]	SPI1_SCK PORTE[13]	SPI1_SCK PORTG[3]	
	TIM[15]	TIM[15] PORTB[2]	TIM[15] PORTD[15]		
PORTB[14]	SPI_SSELBn[2]	SPI1_SSn2 PORTG[5]			
	SPI_MOSIB	SPI1_MOSI PORTC[11]	SPI1_MOSI PORTE[15]		
	TIM[14]	TIM[14] PORTB[3]	TIM[14] PORTD[14]		

VA10820 Port pin default function	VA10820 Special Functions	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO
PORTB[13]	SPI_SSELBn[3]	SPI1_SS _n 3 PORTB[4]	SPI1_SS _n 3 PORTE[9]	SPI1_SS _n 3 PORTG[4]	
	SPI_MISOB	SPI1_MISO PORTC[10]	SPI1_MISO PORTE[14]	SPI1_MISO PORTG[4]	
	TIM[13]	TIM[13] PORTB[4]	TIM[13] PORTD[13]		
PORTB[12]	SPI_SSELBn[4]	SPI_SS _n 4 PORTB[3]	SPI_SS _n 4 PORTE[8]		
	SPI_SSELBn[0]	SPI1_SS _n 0 PORTC[8]	SPI1_SS _n 0 PORTE[12]	SPI1_SS _n 0 PORTE[2]	
	TIM[12]	TIM[12] PORTD[12]	TIM[12] PORTF[12]	TIM[12] PORTG[6]	
PORTB[11]	SPI_SSELBn[5]	SPI1_SS _n 5 PORTB[2]			
	SPI_SSELBn[1]	SPI1_SS _n 1 PORTC[7]	SPI1_SS _n 1 PORTG[6]		
	TIM[11]	TIM[11] PORTD[11]	TIM[11] PORTF[11]		
PORTB[10]	SPI_SSELBn[6]	SPI1_SS _n 6 PORTB[1]			
	SPI_SSELBn[2]	SPI1_SS _n 2 PORTG[5]			
	TIM[10]	TIM[10] PORTD[10]	TIM[10] PORTF[10]	TIM[10] PORTG[3]	
PORTB[9]	UARTA_TX	UART0_TX PORTA[2]	UART0_TX PORTC[4]	UART0_TX PORTE[2]	UART0_TX PORTG[0]
	SPI_SCKA	SPI0_SCK PORTB[15]			
	SPI_SSELCn[1]	SPI2_SS _n 1 PORTA[3]			
PORTB[8]	UARTA_RX	UART0_RX PORTA[3]	UART0_RX PORTC[5]	UART0_RX PORTE[3]	UART0_RX PORTG[1]
	SPI_MOSIA	SPI0_MOSI PORTC[1]			
	SPI_SSELCn[2]	SPI2_SS _n 2 PORTA[2]			
PORTB[7]	UARTB_TX	UART1_TX PORTB[14]	UART1_TX PORTD[11]	UART1_TX PORTF[12]	
	SPI_MISOA	SPI0_MISO PORTC[0]			
	SPI_SSELCn[3]	SPI2_SS _n 3 PORTA[1]			
PORTB[6]	UARTB_RX	UART1_RX PORTB[15]	UART1_RX PORTD[12]	UART1_RX PORTF[13]	
	SPI_SSELAN[0]	SPI0_SS _n 0 PORTB[14]			
	TIM[6]	TIM[6] PORTA[6]			
PORTB[5]	SPI_SCKB	SPI1_SCK PORTC[9]	SPI1_SCK PORTE[13]	SPI1_SCK PORTG[3]	
	SPI_SSELAN[6]	No equivalent SS _n function on VA41628 SPI0 – SPI1 could be used			
	TIM[5]	TIM[5] PORTA[5]	TIM[5] PORTB[12]		
PORTB[4]	SPI_MOSIB	SPI1_MOSI PORTC[11]	SPI1_MOSI PORTE[15]		

VA10820 Port pin default function	VA10820 Special Functions	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO	The same function can be found on VA41628 GPIO
	SPI_SSELAN[5]	No equivalent SSn function on VA41628 SPI0 – SPI1 could be used			
	TIM[4]	TIM[4] PORTA[4]	TIM[4] PORTB[13]		
PORTB[3]	SPI_MISOB	SPI1_MISO PORTC[10]	SPI1_MISO PORTE[14]	SPI1_MISO PORTG[4]	
	SPI_SSELAN[4]	No equivalent SSn function on VA41628 SPI0 – SPI1 could be used			
	TIM[3]	TIM[3] PORTA[3]	TIM[3] PORTB[14]		
PORTB[2]	SPI_SSELBn[0]	SPI1_SS0 PORTC[8]	SPI1_SS0 PORTE[12]	SPI1_SS0 PORTE[2]	
	SPI_SSELAN[3]	No equivalent SSn function on VA41628 SPI0 – SPI1 could be used			
	TIM[2]	TIM[2] PORTA[2]	TIM[2] PORTB[15]		
PORTB[1]	SPI_SSELBn[1]	SPI1_SS1 PORTC[7]	SPI1_SS1 PORTG[6]		
	SPI_SSELAN[2]	SPI0_SS2 PORTB[12]			
	TIM[1]	TIM[1] PORTA[1]	TIM[1] PORTC[0]	TIM[1] PORTF[1]	
PORTB[0]	SPI_SSELBn[2]	SPI1_SS2 PORTG[5]			
	SPI_SSELAN[1]	SPI0_SS1 PORTB[13]			
	TIM[0]	TIM[0] PORTA[0]	TIM[0] PORTC[1]	TIM[0] PORTF[0]	

7. Register Names That Have Changed (need to be changed in user code)

7.1. Timers

Replace occurrences of 'TIM_PERIPHERAL' with 'TIM' (register bit masks).

Replace 'VOR_TIM->BANK[x].EXAMPLE_REG' with 'VOR_TIM_BANK[x]->EXAMPLE_REG'. Bank access has changed due to timers residing on different APB busses.

7.2. UART

Replace occurrences of 'UART_PERIPHERAL' with 'UART' (register bit masks).

Replace occurrences of 'UARTA' with 'UART0', 'UARTB' with 'UART1'.

On the VA41628, there is a third UART available (UART2). Some GPIO pins that mapped to UART0 or 1 on the VA10820 may map to UART2 on the VA41628. On the VA41628, UART2 runs at a different clock rate than UART0 and UART1, because it resides on a different APB bus. UART0 and 1 are clocked by APB2 clock at SYSCLK/4, UART2 is clocked by APB1 clock (SYSCLK/2). This will change baud rate calculations slightly.

7.3. SPI

The Boot ROM SPI on the VA41628 is SPI3, on the VA10820 it is SPIC. References to SPIA, B, C in the code should be replaced with SPI0, 1, 2, or 3. Replace 'SPix_DATA_BMSTOP_Msk' with 'SPix_DATA_BMSTART_BMSTOP_Msk'. On the VA41628, the SPI peripherals are clocked by ½ the system clock, this is different from the VA10820 where the SPI peripheral is clocked by system clock. Here are the changes made to an example function:

```
292 unsigned long M95M01_Read(unsigned long adr, unsigned long sz, unsigned char *buf)
293 {
294     int32_t i ;
295     volatile unsigned char readVal ;
296
297     M95M01_wait_WIP();
298     M95M01_wait_idle();
299
300     VOR_SPI->BANK[3].DATA = READ; // Read command
301     VOR_SPI->BANK[3].DATA = MSB_ADDR_BYTE(adr); // Address high byte
302     VOR_SPI->BANK[3].DATA = MID_ADDR_BYTE(adr); // Address mid byte
303     VOR_SPI->BANK[3].DATA = LSB_ADDR_BYTE(adr); // Address low byte
304
305     for( i=0; i<4; i++ ) {
306         VOR_SPI->BANK[3].DATA = 0x00; // Pump the SPI
307         while( !(VOR_SPI->BANK[3].STATUS & SPI3_STATUS_RNE_Msk) ) { };
308         readVal = VOR_SPI->BANK[3].DATA; // Void read
309     }
310
311     for( i=0; i<sz; i++ ) {
312         VOR_SPI->BANK[3].DATA = 0x00; // Pump the SPI
313         while( !(VOR_SPI->BANK[3].STATUS & SPI3_STATUS_RNE_Msk) ) { };
314         *buf = VOR_SPI->BANK[3].DATA;
315         buf++;
316     }
317     VOR_SPI->BANK[3].DATA = SPI3_DATA_BMSTART_BMSTOP_Msk; // Terminate Block Transfer
318     M95M01_wait_idle();
319
320     return(adr+sz);
321 }
```

Replace all occurrences of 'VOR_SPI_PERIPHERAL_TYPE' with 'VOR_SPI_TYPE' (register bit masks).

7.4. I2C

Replace occurrences of 'I2C_PERIPHERAL' with 'I2C' (register bit masks).

Replace occurrences of 'I2CA' with 'I2C0', 'I2CB' with 'I2C1'.

7.5. Interrupts

Some of the interrupt IRQ numbers have changed, by referencing the VA416xx header file instead of the VA10820 header, these should be fixed, but be aware that some special attention is to be paid here since the Cortex-M4 has many more IRQs than the Cortex-M0.

7.6. Watchdog

One of the 24 timers in the VA10820 is used as the watchdog (routed to WDT_RESET). In the VA41628, dedicated watchdog hardware is available. This watchdog setup is provided in the template VA41628 project, it is enabled by defining ENABLE_WATCHDOG in board.h.

8. Additional Features Available

The VA41628 has a DMA engine. User code can be modified to take advantage of the DMA not present on the VA10820. The VA41628 has a hardware single precision floating point unit (FPU), this will accelerate floating point operations. The FPU is enabled by default in the template project. The VA41628 also has a bit-banding memory region, accelerating some bitwise memory operations.