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Radiation Testing Report: Vorago VA10820

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Abstract

This report contains a collection of empirical data on space radiation effects on the Vorago VA10820 radiation-hardened microcontroller. During testing which occurred on April 5, 2018 at the BASE Facility at the Lawrence Berkeley Lab, the device was subjected to approximately 316K rad(Si) of proton radiation. The results of the proton test were satisfactory, with several key figures-of-merit confirmed empirically. Further testing was performed on June 22-23, 2018 at the BASE Facility, where the device was subjected to a cocktail of heavy ions. From the results, a Weibull LET curve can be produced in addition to notes on other qualitative behavior.

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1 Introduction

The Vorago VA10820 is a microcontroller with an Arm Cortex-M0 CPU, designed for use in extreme temperature or radiation environments. The VA10820 is marketed as having latchup immunity, withstanding a minimum of 300K rad(Si) of ionizing radiation [1].

Given the vendor's impressive claims in their marketing documentation, The Aerospace Corporation has taken an interest in verifying the claims empirically. The hope is that these test results will help inform the Aerospace engineering community about any risks with leveraging the VA10820 in future designs.

2 Component Overview

The VA10820 is functionally similar to commercially available microcontrollers with Arm Cortex-M0 CPUs through its inclusion of popular interface busses and industry standard components. The block diagram below shows the components present within the VA10820.

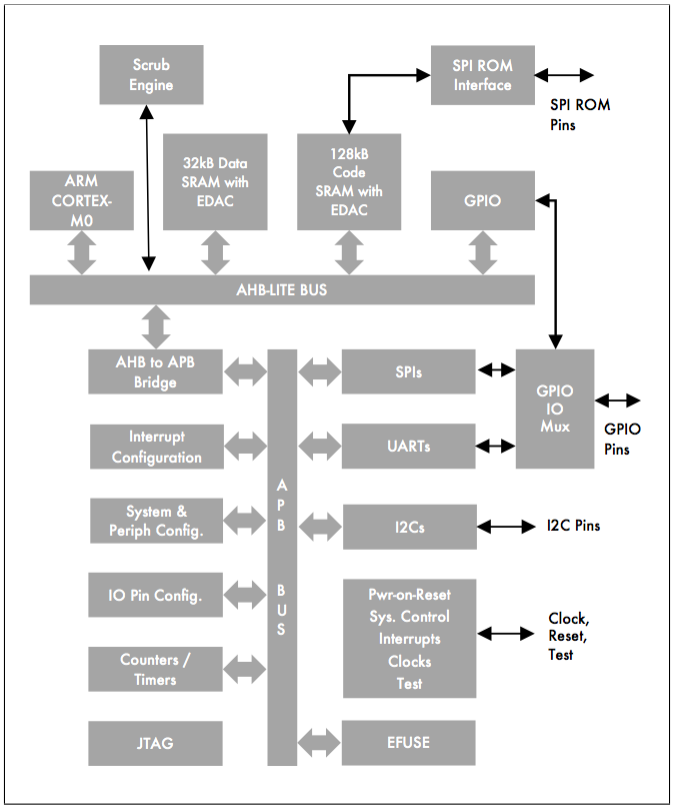

Figure 1: *VA10820 block diagram*

There are several enabling technologies that harden the part against deleterious radiation effects, which makes the VA10820 attractive to use in space applications over standard COTS microcontrollers. The enabling technologies within the VA10820 are:

- Buried Ground Ring layer

- Triple Modularly Redundant registers
- Dual-Interlocked Storage Cell latches
- Error Detection and Correction with scrubbing

2.1 Error Detection and Correction (EDAC)

Memory error correction schemes can be characterized using numerous metrics. One metric that is published frequently is uncorrectable bit error rate, or UBER [2].

To minimize the UBER, the VA10820 MCU utilizes an error detection and correction (EDAC) engine on all of its SRAMs. Through the use of a 20-bit EDAC codeword [3], the MCU has the ability to correct a single bit error or detect a multiple bit error (SECDED) within an 8-bit byte.

2.1.1 Analysis

The programmer's guide [3] provides some details about the EDAC implementation. The guide mentions certain important parameters which can help guide an in-depth analysis of the error detection and correction power of the MCU. The VA10820 register map contains several registers that enable designers to encode/decode data using the EDAC engine. More specifically, Section 4.4.6 states the following:

> The SYND END 32_52 register provides read access to the 32/52 EDAC Syndrome encoder. The output is a 20 bit EDAC code word generated from bits 31:0 of the SYND_DATA0 register value. This is the EDAC code word used on VORAGO parts VA10800/VA10820 and GLM003A/GLM004A for internal memory. The 20 bit code is composed of 4 - 5 bit syndromes generated for each 8 bits of the input data.

Using this functionality, one can perform a non-exhaustive cursory check of the coding algorithm.

1. The SYND_DATA0 output for the 32-bit machine word 32'h00000055 is 32'h00000017. The parity bits for least significant byte are located at [4:0]. The bits are: 5'b10111.
2. The SYND_DATA0 output for the 32-bit machine word 32'h55000000 is 32'h000b8000. The parity bits for the most significant byte are located at [19:15]. The bits are: 5'b10111.

The documentation and behavior of the EDAC test registers suggest that the ECC used is Hamming(13,8), or Hamming(12,8) with an additional parity bit. The Hamming(12,8) generator matrix is

$$G = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \end{bmatrix}$$

and associated parity-check matrix H

$$H = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

The codeword of the test byte used earlier (8'h55) can be computed as follows

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} 0 \\ 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 0 \\ 1 \end{bmatrix} = \begin{bmatrix} d_7 \\ d_6 \\ d_5 \\ d_4 \\ d_3 \\ d_2 \\ d_1 \\ d_0 \\ p_3 \\ p_2 \\ p_1 \\ p_0 \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ \mathbf{0} \\ \mathbf{1} \\ \mathbf{1} \\ \mathbf{1} \end{bmatrix}$$

Let p_4 be an additional parity bit, or the mod-2 sum of the codeword. This would yield $p_4 = 1$. The full syndrome would then be

$$\begin{bmatrix} p_4 \\ p_3 \\ p_2 \\ p_1 \\ p_0 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 1 \\ 1 \\ 1 \end{bmatrix}$$

This parity word matches the syndrome bits generated by the VA10820. Although this analysis does not serve as a formal proof, nor is it a replacement for exhaustive checking or RTL IP inspection, it appears that the EDAC ECC algorithm used is Hamming(13,8).

3 Methodology

This section's information about the supporting hardware used during the testing, as well as a description of the actual test flow, is enumerated.

3.1 Preparation

3.1.1 Protons

The following test flow was followed for the proton radiation testing on April 5, 2018.

1. Unpack Pelican case. The contents of the case should be as follows:
    - 1x Vorago REB1-VA10820
    - Instrumentation amplifier box w/ SMA-M pigtail attached
    - AC/DC +9V switcher w/ SMA-M pigtail attached
    - DB-9 GPIO pigtail for the CAVE
    - DB-9 GPIO pigtail for the upstream Saleae

- Saleae Logic Pro 16
- USB 3 cable for the Saleae
- Macbook with Python test scripts
- Stash of misc. gender changers for all cables
- Soldering iron + other rework equipment (for emergencies)

2. Collect additional equipment brought for testing. This includes:
   - 2x output power supply
   - Oscilloscope
3. Install the REB1-VA10820, along with the instrumentation amplifier and GPIO DB-9 pigtail, in the cave as noted in Figure 4.
4. Connect USB, BNC, and DB-9 from cable bundle to REB1-VA10820.
5. Run the cable bundle through the feedthrough, up to the control room.

3.1.2 Heavy Ions

The following test flow was followed for the heavy ion radiation testing on June 22, 2018.

1. Unpack Pelican case. The contents of the case should be as follows:
   - 3x Vorago REB1-VA10820 with delidded IC at U5
   - Macbook with Python test scripts
   - Stash of misc. gender changers for all cables
   - Soldering iron + other rework equipment (for emergencies)
2. Collect additional equipment brought for testing. This includes:
   - 4x output power supply
3. Install the REB1-VA10820 in the vacuum chamber as noted in Figure 5.
4. Connect USB and BNC to internal vacuum chamber connectors.
5. Connect cable bundle to matching external vacuum chamber connectors.
6. Run the cable bundle through the feedthrough, up to the control room.

3.2 Chamber Details

3.2.1 Protons

Cave 4A was used to dose the DUT with protons. Since protons can penetrate ordinary device packaging, a 1" collimator was used to localize the beam around the VA10820 IC. Figure 2 shows the post-processed analysis of the Gafchromic film which was subjected to the tuned proton beam.

Table 1: *Proton beam parameters*

Parameter	Description	Nominal Value	Units
Fluence	Total particles through unit area	TBD	$\frac{protons}{cm^2}$
Flux	Fluence per unit time	1.0×10^8 (1e8)	$\frac{protons}{s.cm^2}$
Energy	Unit of energy for proton after acceleration through cyclotron	50	MeV

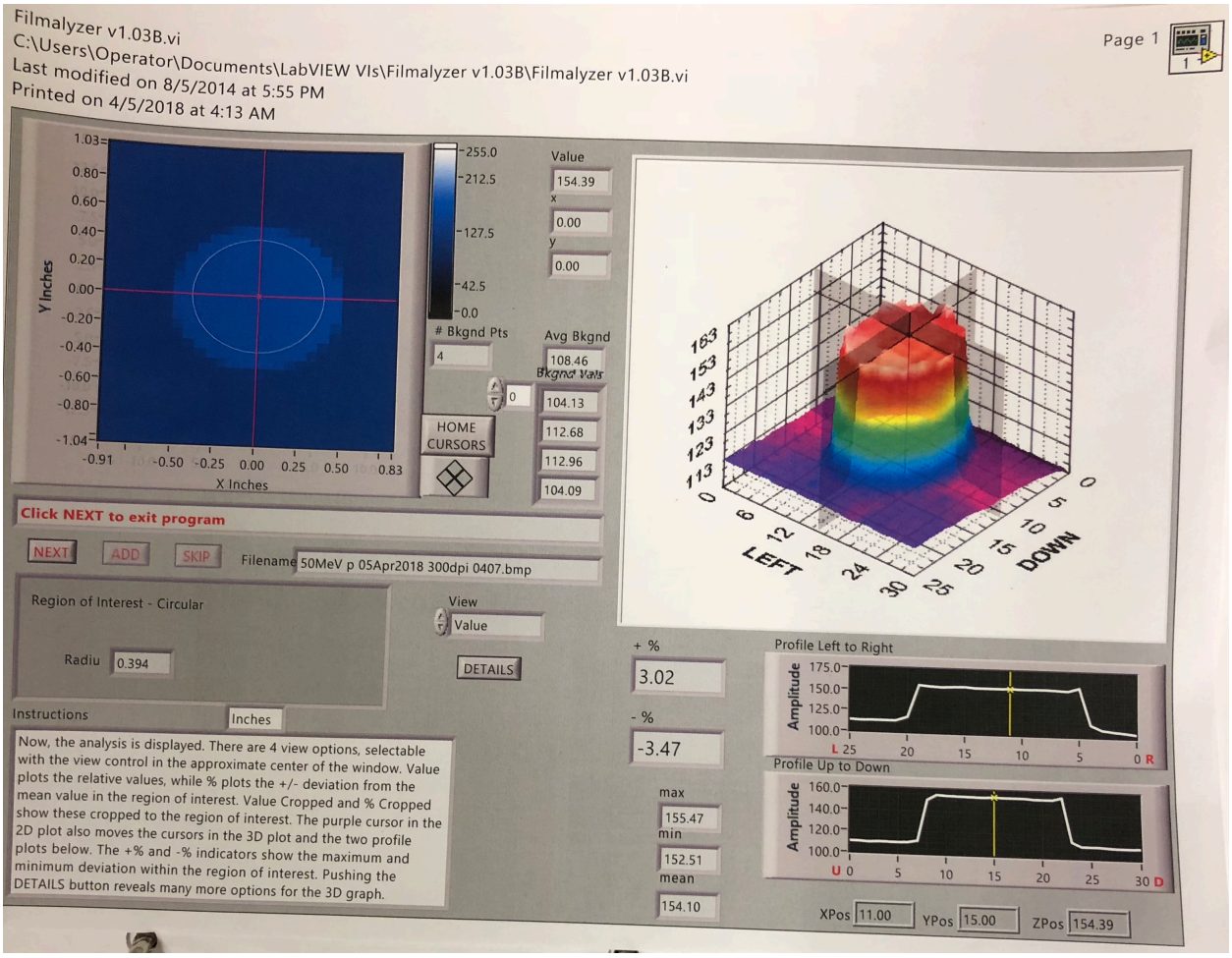

Figure 2: *Photo of analysis results of beam test film in chamber*

Table 1 enumerates the proton beam tuning parameters. Several of these parameters are considered nominal, and thus are being actively monitored by the source operator.

The desired beam angle of incidence onto the DUT is 0°.

3.2.2 Heavy Ions

Cave 4B was used to dose the DUTs with heavy ions.

The BASE facility provides a selection of heavy ion cocktails with varying energies. For the heavy ion test, the 10 MeV/nucleon cocktail is used. Table 2 enumerates the LET for each element used for testing, with a 0° angle of incidence:

Table 2: *Ion to LET*

Ion	$^{11}_{5}\mathbf{B}$	$^{18}_{8}\mathbf{O}$	$^{22}_{10}\mathbf{Ne}$	$^{29}_{14}\mathbf{Si}$	$^{40}_{18}\mathbf{Ar}$	$^{65}_{29}\mathbf{Cu}$	$^{86}_{36}\mathbf{Kr}$	$^{124}_{54}\mathbf{Xe}$
LET	0.89	2.19	3.49	6.09	9.74	21.17	30.86	58.78

See [4] for more information.

3.2.3 Photos

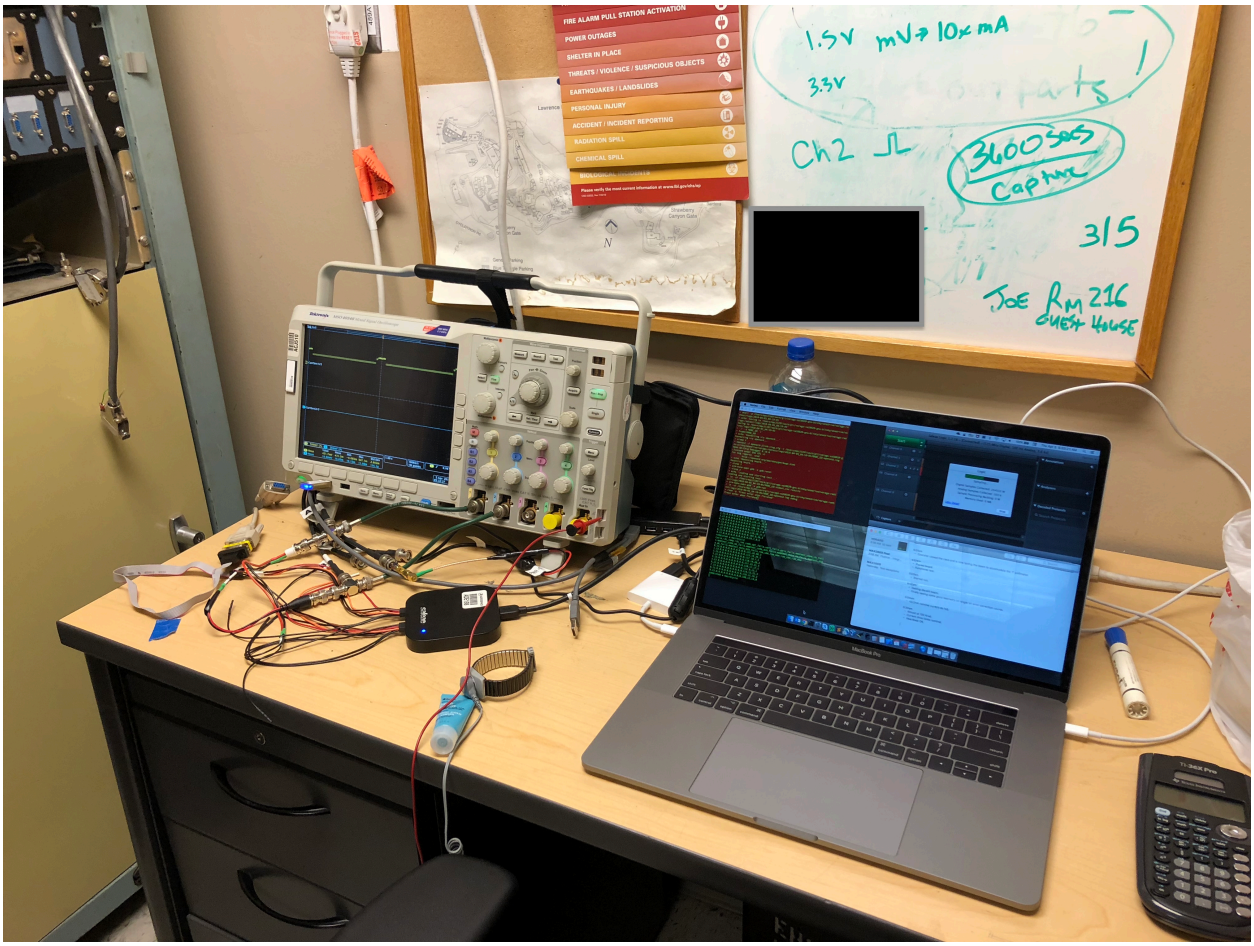

Figure 3: *Photo of oscilloscope and laptop in control room*

3.3 Procedure

3.3.1 Protons

Prior to starting the beam, initialize the test automation script. The script loads the test firmware onto the VA10820 via JTAG. Afterwards, the logic analyzer internal trigger is armed to await a trigger signal from

the DUT. At this point the DUT is ready to be subjected to the proton beam. While the beam is running, the test operator monitors all observable data streams for anomalies. The test operator will restart the test automation software after every hour of beam time.

3.3.2 Heavy Ions

At the start of a given ion run in the cocktail, the test operator starts the test automation script. Similar to the process used for protons, the test operator actively monitors all observable data streams for anomalies. Each ion is tested a minimum of 3 times for each DUT, with the beam on for 120 seconds. The run results are saved separately in a CSV file.

3.4 Teardown

1. Notify the operator to open the cave.
2. (Everything after here should be coordinated with operator as irradiated equipment could be hot).
3. Disconnect cables from DUT.
4. Use meter to determine parts which require long-term storage due to excessive radiation activation.

4 Figures of Merit

Table 3 lists the figures of merit published by Vorago. For additional context, see [5].

Table 3: *VA10820 radiation figures-of-merit*

Parameter	Description	Min	Max	Unit
TID	Total Ionizing Dose	300K	-	rad(Si)
SER	Soft Error Rate (EDAC off)	-	1.3×10^{-7}	errors/bit/day [1]
SER	Soft Error Rate (EDAC on)	-	1.0×10^{-15}	errors/bit/day [1]
LET	Linear Energy Transfer	110	-	$\frac{MeV-cm^2}{mg}$
SEFI	Single Event Functional Interrupt	-	1.0×10^{-9}	upsets/device/day [1]

5 LBL 88-inch Cyclotron Facility

Device characterization was conducted using the 88-inch Cyclotron, located at Lawrence Berkeley Laboratory in Berkeley, CA. Aerospace uses the Berkeley Accelerator Space Effects (BASE) facility to perform space radiation experiments and device qualification.

Cave 4A was used to subject the VA10820 ASIC to protons. Cave 4B was used to subject the VA10820 ASIC to heavy ions.

Mr. M. Carino, Mr. S. Snow, and Dr. S. Davis were present to execute fixture setup in the cave for proton testing, monitor the beam and observe DUT parameters in the control area while radiation was active, and subsequent teardown.

For heavy ion testing, Mr. S. Snow, Dr. S. Davis, Dr. J. George, and Dr. R. Koga were present at various time intervals during testing to execute fixture setup monitor the beam, run the test software, and perform teardown.

[1] At geosynchronous solar min with 100 mils of aluminum shielding

6 Instrumentation

Figure 4 and Figure 5 gives an overview of the test instrumentation used to interface with the DUT during irradiation for proton and heavy ion testing, respectively.

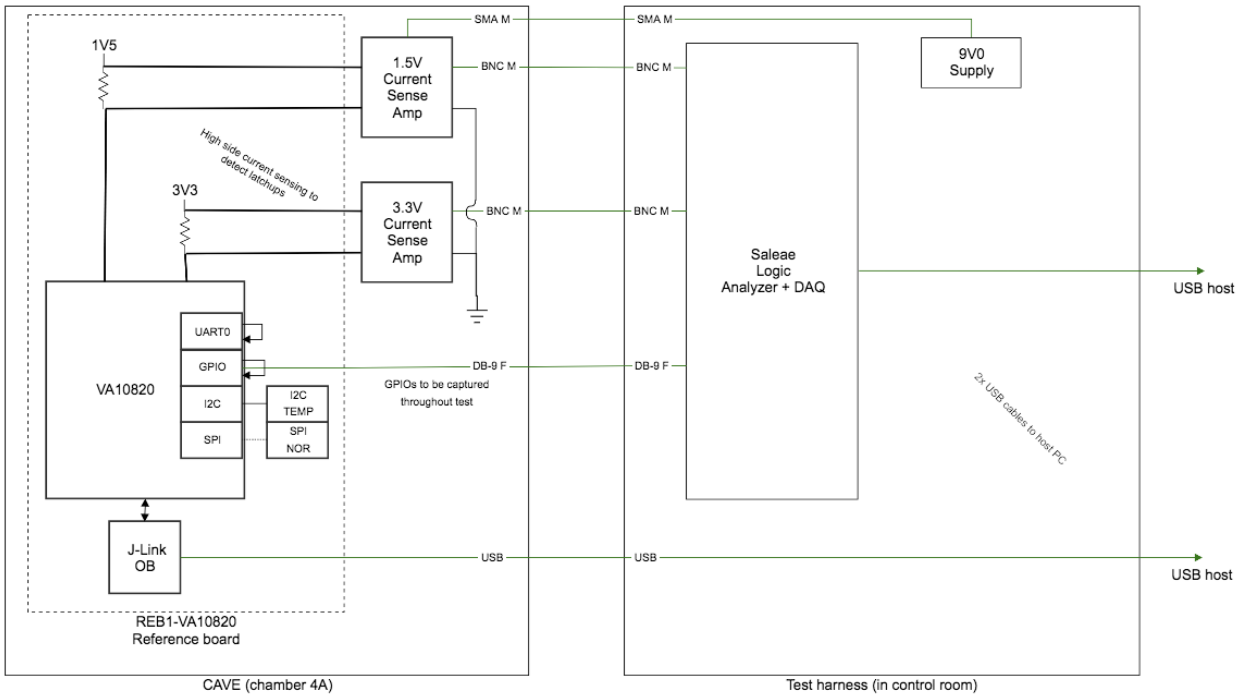

Figure 4: *Wiring diagram of the proton test fixture*

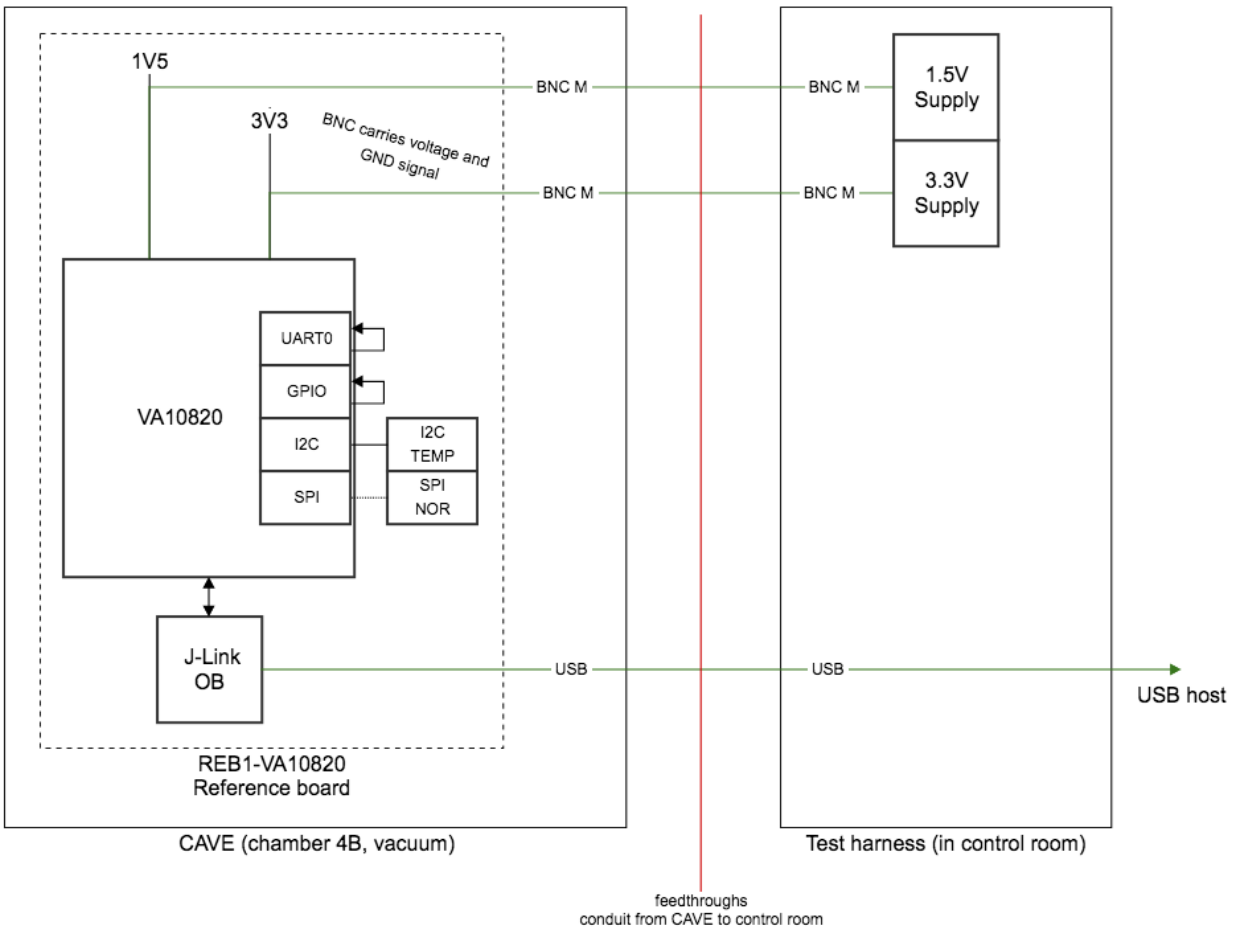

Figure 5: *Wiring diagram of the heavy ion test fixture*

7 Test Software

Software testing is used in order to confirm the *radiation hardened* feature of the VA10820. Table 4 provides a summary of the components tested, as well the subset of the total component space used for testing.

Table 4: *Components tested*

Component	Available	Tested	Notes
Memory	128KB code, 32KB data	8KB code, 8KB data	EDAC as well
GPIO	2 GPIO Ports, 54 pins total	2 input, 2 output pins	Port B
SPI	3 interfaces	1 interface	SPIC
UART	2 interfaces	1 interface	UARTA
I2C	2 interfaces	1 interface	I2CA

7.1 Memory Testing

In order to verify that the integrity of the memory is maintained, 8KB blocks in both code and data memory regions are allocated and tested. Dynamic memory testing is performed by writing and reading back various

patterns throughout the test region. Several algorithms of various fault coverage are employed to check for memory faults (Table 5) [6].

Table 5: *Memory testing algorithms*

Algorithm	Address Fault	Stuck-at Fault	Transition Fault	Coupling Fault
Checkerboard	-	Locate	-	-
Walking 1/0	Locate	Locate	Locate	Locate
March C-	Detect	Detect	Detect	Detect

Additionally, EDAC registers are periodically sampled, indicating the number of addresses exhibiting either single bit errors (SBE) or multiple bit errors (MBE) in both the code and data memory.

An SBE can be corrected with the memory scrubber, which fixes one SBE per cycle. An MBE is only correctable with a soft reset. For testing, the code memory (ROM) and data memory (RAM) scrubbers are configured to run at 500 Hz (one memory address scrubbed every 2 ms). During vendor testing, this scrub rate resulted in an SER surpassing product specification [7].

7.1.1 Faults

Address Fault: Address decoder issue where memory cannot be accessed properly.
Stuck-at Fault: Cell is stuck at a particular value.
Transition Fault: Cell does not transition between 1 and 0 correctly.
Coupling Fault: Writing one cell writes to another adjacent cell as well.

7.1.2 Algorithms

Checkerboard: The checkerboard test works by applying a 0101... pattern to a region of memory, reading back that memory (checking for errors), and then repeating that process with the anti-pattern (i.e. 1010...). Each fault is recorded per 1-byte address where the pattern could not be verified.
Walking 1/0: The walking 1/0 test alternates between pushing a 1 value through a 0-filled memory and, conversely, a 0 value through a 1-filled memory. After each write to the memory word, the address is read back to confirm a proper write. Each fault is recorded per 1-byte address where a bit failed to "walk" across all 8 bits.
March C-: The march test performs a sequence in which a 0 or 1 is written to all memory locations, then the values are verified at these locations (the opposite value is written in the process). This sequence is performed several times in different addressing orders. There are several different variations of this test, but the chosen one (March C-) is commonly used and performs the following sequence: up(write 0), up(read 0,write 1), up(read 1,write 0), down(read 0,write 1), down(read 1,write 0), up(read 0). Each fault is recorded per bit per traversal where the expected value could not be verified.

7.2 Peripherals

The peripherals are tested to ensure that none of the modules on the chip are particularly vulnerable to radiation.

7.2.1 GPIO

The GPIO test is performed on a set of pins that loop through a pattern. The results are verified both externally using a logic analyzer, as well as internally by having input-configured pins on the board read the outputs.

For the test, 4 adjacent pins are chosen from the headers, 2 configured as input and 2 as output. Each input is soldered on the underside of the board to the adjacent output to form a loopback. Table 6 describes the configuration.

Table 6: *GPIO configuration*

Label	Header	Pin	Mode
PORTB_18	J14	9	OUT
PORTB_19	J14	10	IN
PORTB_20	J14	11	OUT
PORTB_21	J14	12	IN

The two output pins are programmed to cycle through the bit pattern 00, 10, 11, 01, moving through a 2-bit Gray code. After each of these outputs are written, the input pins read the data and compare it to the expected pattern. Each fault is recorded per pin per read that could not be properly verified.

Additionally, the two outputs are read by the Saleae Logic16 logic analyzer and recorded to a file for offline analysis.

7.2.2 SPI

SPI is tested by writing to and reading from the onboard SPI flash memory. To ensure a diverse range of values tested, a 16-bit linear feedback shift register is used with an arbitrary starting seed. This pseudo-random series of values is written to the first 64 bytes of flash, and then read back to verify. Each fault is recorded per 2-byte location in memory with an invalid read.

7.2.3 UART

The UART is tested with an external loopback test. This is achieved by using a jumper wire to connect external pins 7 (UARTA_TX) and 8 (UARTA_RX) on J10 with the GPIO pins properly pin-muxed. Similar to the SPI test, an 8-bit linear feedback shift register is used to generate 16 pseudorandom characters per cycle to write to the 16-byte FIFO buffer. Afterwards, the 16 characters are read back to verify that the data was transmitted properly. Each fault is recorded per character improperly transmitted.

7.2.4 I2C

In order to reduce the number of separate devices to connect on the test rig, the on-board temperature sensor (ADT75) is used, which communicates a temperature reading to the VA10820 via I2C channel A. In case of I2C failure, the request would not be valid, or the data received would not be properly decoded by the I2C module. As a metric, the return code and the temperature were recorded during the test.

7.3 Test Suites

7.3.1 Functional: Protons

This test suite contains all of the memory and peripheral tests. The purpose is to see if any faults occur due to the build up of radiation over time from protons. There is a neglible delay between writes and reads in memory testing, similar to standard memory testing software (e.g. memtest86). Both code and data SRAM were tested, with a 500 Hz scrub rate.

The non-delidded DUT underwent this test suite during proton testing.

7.3.2 Functional: Heavy Ions

This test suite is based off of the Functional suite, with slight modifications to the memory testing. In this case, only the checkerboard pattern was tested. Between writes and reads, there is an enforced 1 second delay. The intention is to allow enough time for the ions to create SEUs on the test region.

DUT-1 and DUT-2 underwent this test suite during heavy ion testing.

7.3.3 Cross-section: Heavy Ions

This test suite focuses specifically on determining the number of SEUs resulting from heavy ions, without help from the EDAC scrubber. The results from this test can therefore be used to plot cross-section vs LET in a Weibull curve. This is done by turning off data SRAM scrubbing, maximizing the rate of code SRAM scrubbing, disabling the peripheral tests, and running a series of basic memory tests on the 8KB data SRAM region.

The memory test flow is to clear the EDAC counters, write the pattern to the entire test region, delay 1 second, read back the entire test region, and then store the values in the EDAC counters. This is repeated for 4 patterns to fully exercise the region (all 0s, all 1s, 0101 checkerboard, 1010 anti-checkerboard).

DUT-3 underwent this test suite during heavy ion testing.

8 Results

8.1 Total Ionizing Dose (TID)

8.1.1 Definition

Total radiation administered to the DUT over the course of testing.

8.1.2 Protons

The DUT was subjected to approximately **316K rad(Si)** through the alotted radiation time, which exceeds the minimum specified in Table 3.

8.1.3 Heavy Ions

Over the course of testing, each DUT was subjected to the following total dose:

Table 7: *Heavy ion TID*

DUT	1	2	3
TID (Krad)	2.20	29.7	6.18

It is not obvious that this TID had an adverse effect on any of the DUTs.

8.2 Single Event Latchup (SEL)

8.2.1 Definition

The DUT is considered *latched-up* if all of the following conditions are met:

1. The DUT current consumption rises well above operating levels and is roughly maintained down to a holding voltage, at which point current draw would drop to zero.
2. The DUT shows observable destructive effects.

8.2.2 Protons

The DUT did not exhibit SEL throughout the entire testing procedure.

8.2.3 Heavy Ions

None of the DUTs exhibited SEL throughout the entire testing procedure.
During testing, DUT-2 experienced a high current event where it sustained 210 mA but did not reach the power supply's max current of 500 mA. This occurred when the DUT was subjected to a fluence of 3.28×10^6 from the ion Xe. Due to the power supply used, the voltage could not be gradually dropped to detect a holding voltage, but the device returned to normal behavior after a hard reset and there were no signs of any destructive effects in subsequent runs. Due to both this, and the relatively low current that was jumped to, it is far more likely that this event could be categorized as a SEFI.

8.3 Single Event Functional Interrupt (SEFI)

8.3.1 Definition

The DUT is deemed to have experienced a SEFI if any of these conditions are met:

1. The DUT ceases to report a periodic heartbeat.
2. The DUT ceases normal operation.

8.3.2 Protons

The DUT experienced a fault which required a JTAG reset at approximately **267K rad(Si)**. The symptoms of the observed fault are as follows:

1. The software defined heartbeat was no longer visible.
2. The DUT current consumption on the 1.5V rail was at approximately 27 mA, which did not indicate a latch-up condition.

8.3.3 Heavy Ions

Each of the DUTs encountered several SEFIs over the course of testing. They were most evident by the current consumption on the 1.5V microcontroller rail significantly changing from the typical amount of 50mA. The SEFIs are summarized as follows:

Table 8: *Heavy ion SEFIs*

Run	DUT	Ion	Fluence	Description
67	2	Xe	3.3×10^6	Lost JTAG, could not find MEM-AP to control core. Current rose to 210 mA.
68	2	Xe	5.0×10^6	Lost JTAG, debug region unpowered. Current dropped to 4 mA.
69	2	Xe	1.0×10^7	Lost JTAG, debug region unpowered. Current dropped to 26 mA (idle).
70	2	Xe	1.0×10^7	Lost JTAG, debug region unpowered. Current dropped to 26 mA (idle).

8.4 Debugging Errors

8.4.1 Definition

Although there are no figures of merit related to the debugging errors, there was adverse behavior observed when using the JTAG debugger to program and read semihosted values back from the devices. A debugging error is characterized by any of the following faults:

1. The DUT's debug region becomes unpowered.
2. The DUT fails to report values via semihosting.

3. The DUT loses JTAG connection.
4. The DUT repeats its program loop.

8.4.2 Protons

As mentioned before, DUT experienced a fault which required a JTAG reset at approximately **267K rad(Si)**. The device failed to report values via semihosting.

8.4.3 Heavy Ions

Multiple debugging errors were observed in heavy ion testing and the results can be tabulated as follows:

Table 9: *Heavy ion debug errors*

Run	DUT	Ion	Fluence	Description
66	2	Xe	9.5×10^5	Lost JTAG, debug region unpowered.
67	2	Xe	3.3×10^6	Lost JTAG, could not find MEM-AP to control core. Current rose to 210 mA.
68	2	Xe	5.0×10^6	Lost JTAG, debug region unpowered. Current dropped to 4 mA.
69	2	Xe	1.0×10^7	Lost JTAG, debug region unpowered. Current dropped to 26 mA (idle).
70	2	Xe	1.0×10^7	Lost JTAG, debug region unpowered. Current dropped to 26 mA (idle).
97	3	Cu	3.0×10^5	Program restarted, continued operation.
102	3	Kr	2.0×10^5	Failed to print heartbeat.
103	3	Kr	3.4×10^5	Automatic reset, continued operation.
104	3	Xe	3.4×10^5	Failed to print heartbeat.
106	3	Xe	4.1×10^5	Lost JTAG, debug region unpowered.
108	3	Xe	1.3×10^6	Lost JTAG, invalid ACK in DAP response.
109	3	Xe	1.5×10^6	Failed to print heartbeat.

These errors could be due to the debug region of the DUT being particularly sensitive to radiation, which would not have an impact during normal operation where the board boots from flash and uses UART or SPI for communication (both of which did not exhibit any errors in testing).

8.5 Single Event Upsets (SEU)

8.5.1 Definition

The DUT is designed to detect and correct SEUs in memory through its EDAC block. The test software includes telemetry for Single Bit Error (SBE) and Multiple Bit Error (MBE) in both SRAM sections.

The `ROM_SCRUB` and `RAM_SCRUB` registers allow for the setting of the EDAC scrubbing rate for the code and data SRAMs, respectively.

8.5.2 Protons

Both scrub registers were set to 100000 counts. At a CPU clock of 50 MHz, the effective scrubber rate is 500 Hz, which corresponds to a scrub rate of one memory address every 2 ms. Any corrections made by the scrubber are added to the EDAC counters, so the counters reflect detections and corrections by the user software and the scrubber.

According to [7], the 500 Hz scrub rate used is associated with an uncorrectable errors per bit-day of 2.65e-16 (assuming geosynchronous solar min with 100 mils of aluminum shielding).

The raw results of the telemetry is seen in the following figures.

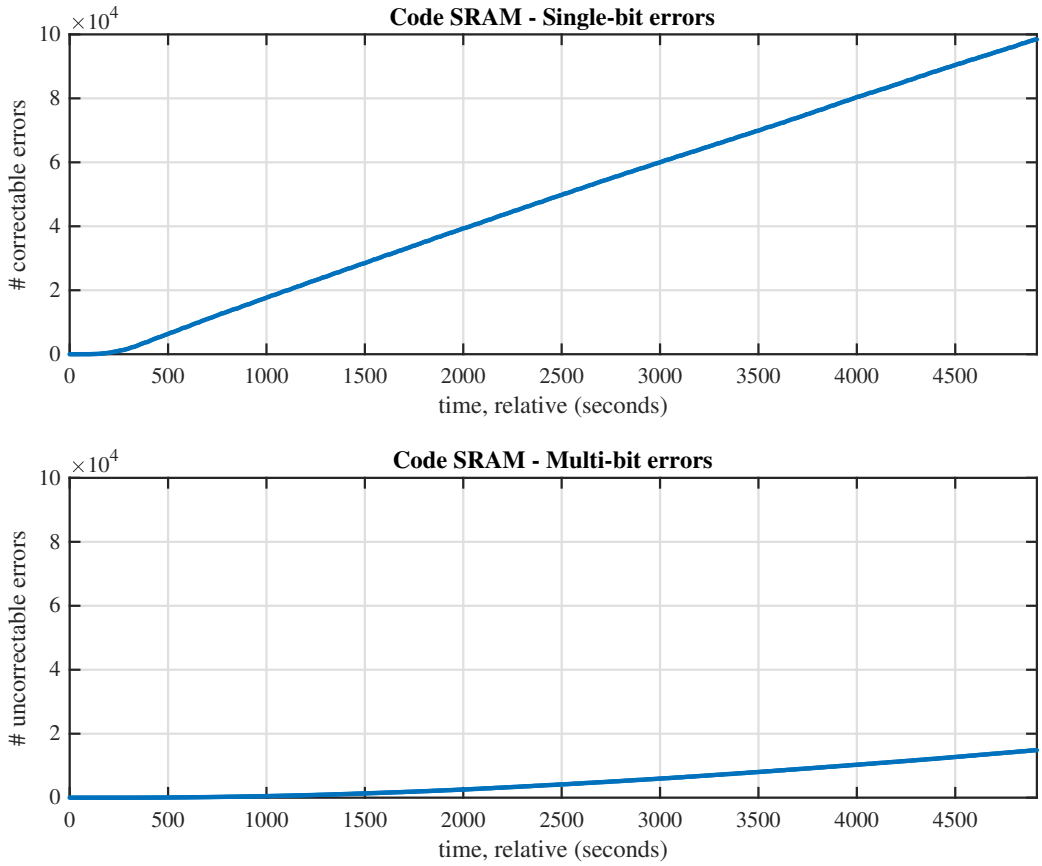

Figure 6: *EDAC scrubber error counters for the code SRAM*

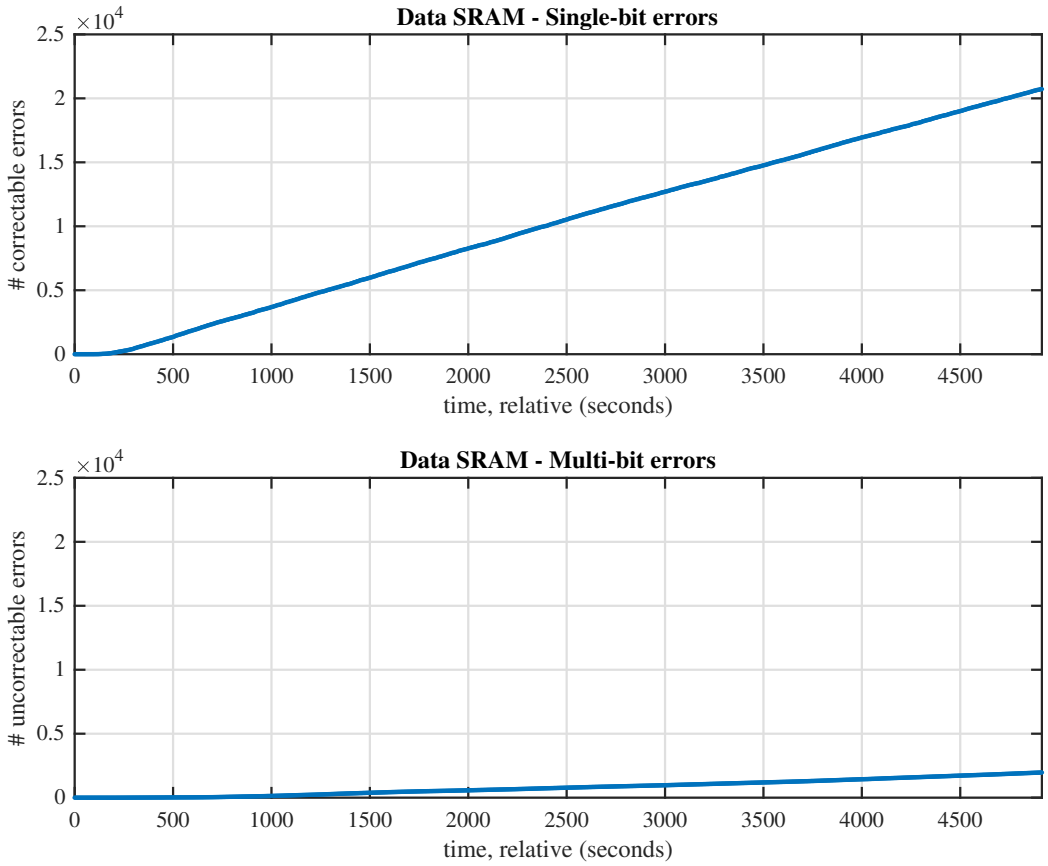

Figure 7: *EDAC scrubber error counters for the data SRAM*

Figure 6 shows the accumlated number of SBEs and MBEs encountered by the EDAC engine. Note the ramp up from 0 to 500 seconds in the single-bit errors, during which the proton flux was increased to a steady-state of 1e8. As evident in Figure 6 and 7, the EDAC and scrubber was functioning during the test.

The error count magnitude differences between the code and data SRAMs are due to the size of the SRAMs. The VA10820 includes 128KB of code SRAM, and 32KB of data SRAM. Thus, one can expect a 4x larger absolute error count in the code SRAM. Figure 8 shows the error counts both SRAMs after taking the SRAM sizes into account.

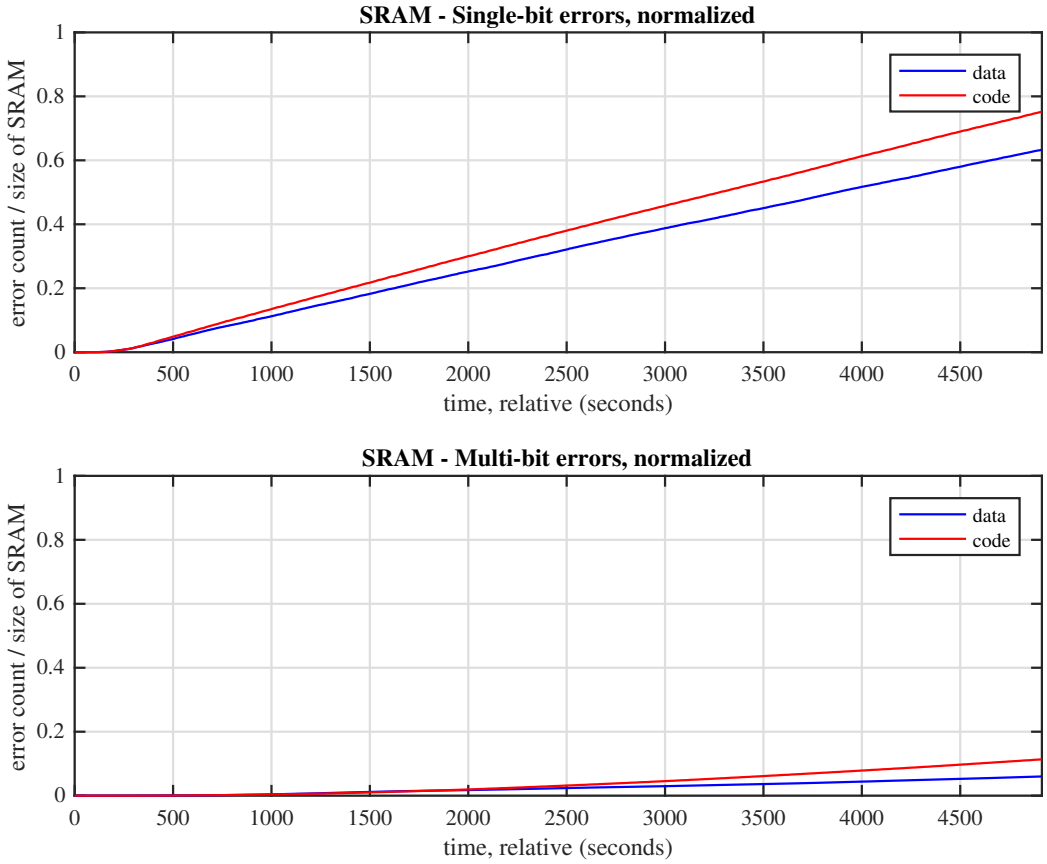

Figure 8: *EDAC error counters for both SRAMs, normalized*

Finally, it is worth reemphasizing that SBEs are corrected on-the-fly by the EDAC, whereas MBEs are uncorrectable. For a typical application, the number of MBEs should be kept at 0. A system designer should adapt the scrub rate to match a mission's radiation profile, and should also design in fault mitigation techniques such as system resets or reinitializations where applicable.

8.5.3 Heavy Ions

The results here focus on the testing for DUT-3, where the cross-section test suite was administered. Here, the SBEs and MBEs result entirely from the user specified reads on the test region, as the data SRAM scrubber is disabled. This allows for a plot to be constructed that shows the relationship between LET and errors.

First, the relevant paramters are calculated for each valid run. Let t_{run} be the duration of the run (i.e. continuous beam time), t_{trial} be the duration of a single trial (i.e. one pass of test software), n be number of errors, d be the duty cycle of the testing, F be the recorded flux, f be the effective fluence, C' be the unscaled cross-section, T be the number of tests per trial (4), B be the number of bytes tested per test (8192), and b be the number of bits tested. Using these values we can generate a cross-section, C, for each LET value.

$$n = SBE_{0s} + SBE_{1s} + SBE_{checker} + SBE_{anti-checker}$$
$$d = \frac{t_{0s} + t_{1s} + t_{checker} + t_{anti-checker}}{t_{trial}}$$
$$f = F \times t_{run} \times d$$
$$C' = \frac{n}{f}$$
$$b = T \times B \times \frac{8bits}{byte}$$
$$C = \frac{C'}{b}$$

Plotting the resulting cross-section against LET we obtain the following Weibull curve fit (Figure 9). We compare our Weibull fit from the error data collected on DUT #3 to the Weibull curve fit determined by Vorago Technologies [7]. Our testing resulted in roughly half as many errors as observed by Vorago Technologies. This discrepancy may have resulted from different testing methodologies, but it would be safe to treat Vorago's Weibull fit (the expected curve) as an upper bound on errors. Table 10 lists the Weibull fit parameters from the observed and expected curves.

Table 10: *Weibull fit parameters*

Parameter	Observed	Expected (Vorago Technologies)
σ_{sat} (cm^2/bit-error)	1.84e-8	3.03e-8
$\text{LET}_{\text{onset}}$ (MeV-cm^2/mg)	8.89e-1	8.89e-1
width	5.35e+1	3.41e+1
exponent	9.68e-1	9.38e-1

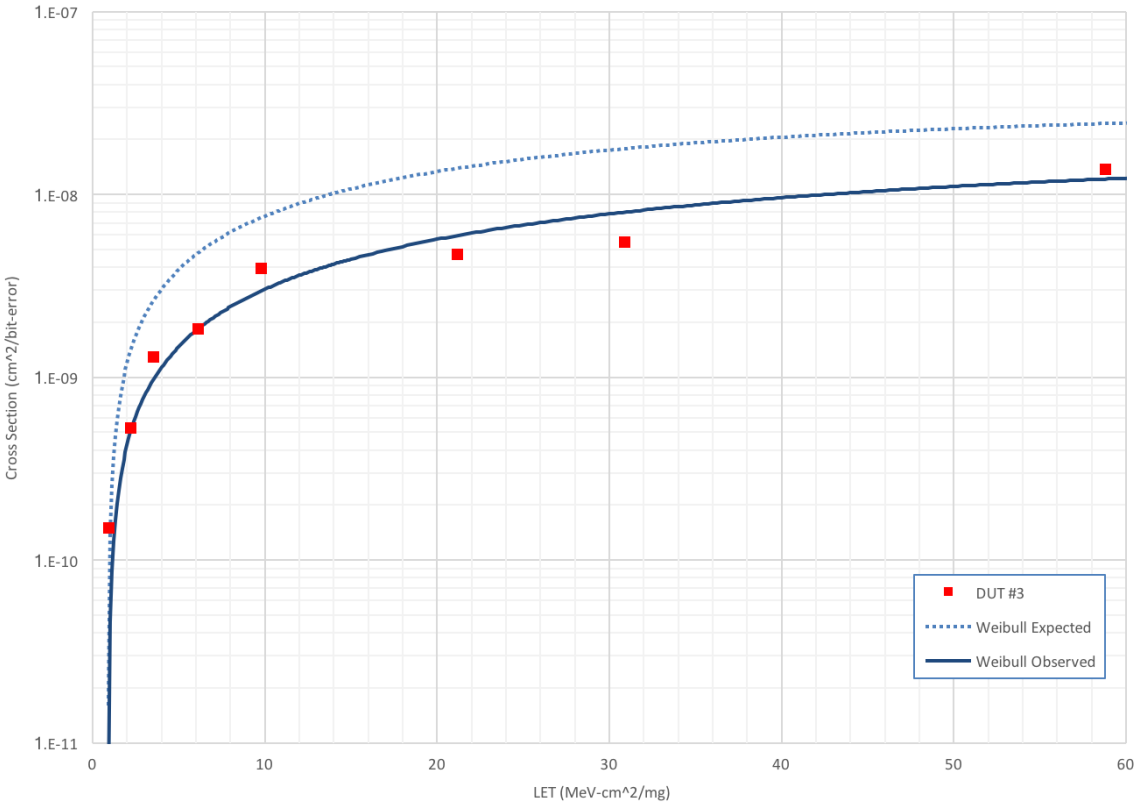

Figure 9: *Weibull curve (no EDAC scrubbing)*

8.6 Miscellaneous

This section contains other various findings of merit during testing.

8.6.1 Code SRAM MBE

Although the documentation for the VA10820 suggests that an MBE should be corrected by a system reset, issuing a reset command over JTAG did not cause code SRAM MBEs to be corrected. This was seen by resetting the board with the beam off and letting the test software run as usual. This behavior was not detected for Data SRAM.

9 Summary

Table 11: *Summary of results*

Parameter	Min	Max	Test Min	Test Max	Units	Result
TID	300K	-	316K	-	rad(Si)	OK
SEL	-	0	-	0	count	OK
SEFI	50	-	58	-	lowest MeV-cm^2/mg with SEFI events	OK

Overall, our results point to the Vorago VA10820 being a resilient board for applications that require a radiation-hardened device. Most of our findings either met or exceeded the findings previously recorded by the Vorago Technologies own radiation testing. The most notable discrepency is in our detection of a high current event at an LET of 58 (not reported by Vorago technologies), but this was likely due to us testing with a higher fluence. None of the DUTs tested entered an unrecoverable state. The memory error rate found indicates that the usage of EDAC scrubbers would be highly effective at limiting bit error rate well below 1e-15 errors/bit-day at Geo solar min with 100 mils of alumnium shielding.

Appendix A Raw Test Journal: Protons

The following is the raw test journal captured by M. Carino for the duration of the test.

4/5/2018

12:21am - Placed reference board into proton cave. - 1.5v and 3.3v sense looks OK. - Saleae digitals look OK.

2:39am - Almost ready to go.

4:01am - Operator closed the cave and is now tuning the beam to accomodate the 1 collimator.

4:57am - Placed board - Functional test.

5:00am - Started run.

5:02am - Getting decent beam. - Finally seeing some good telemetry on single bit error correction counts.

5:04am - 43.2mA nominal current on 1v5.

5:30am - Almost at 100 Krad. - Current draw looks nominal. - Heartbeat OK.

5:46am - 150 Krad - All signals nominal.

5:59am - Preparing to save Saleae capture and restart.

6:00am - Restarted capture.

6:02am - All signals still look nominal. No fatal error counts. - 200 krad.

6:14am - All signals nominal. No fatal error counts.

6:17am - 250 krad.

6:23am - 267 krad. - Observed drop in current, flat line. - Halted beam. - Reset chip, no power cycle. - Seemed to halt at 27.x mA

6:26am - Restarted beam.

6:37am - LabView notes that we just hit 300 krad. - We will continue to 311 so that it matches the fluence. Currently at 2.11e11.

6:43am - Halted beam. - Approx 316 krad applied to part.

Appendix B Raw Test Journal: Heavy Ions

The following is the raw test journal captured by S. Snow for the duration of the test.

Vorago radtest 6/22 4:43 PM

PRE-TEST Logs leading up in juneprep

Used gray usb cable. Had one issue with usb connection lost with openocd. Tested a few more times and didnt occur again.

Using silver usb cable.

Changes: Not using saleae, just looking at current use and reported logs. Only connections coming out are USB, 3V3(with GND) and 1V5(with GND)

Current limit at 100mA for both 1 and 2. Nominal avg is 22mA with 3V3 and 27mA at rest and 53mA at load for 1V5

4:48 - Final prep tests complete. Request Rocky to close chamber.

4:49 - Chamber closing.

4:50 - While chamber closing, current draws changed to 30mA for 3V3 and 24mA for 1V5

4:52 - Ran abbreviated test chamber-closing and now currents are back to normal.

5:05 - Rocky encountered issue closing chamber.

5:07 - (chamber-closed2) occasionally getting annoying error: "Error: Failed to send data to device: LIBUSB_ERROR_NO_DEVICE. Error: transport_write() failed: unspecified error. Error: jaylink_jtag_io() failed: JAYLINK_ERR." Might have to ignore this issue during the test.

5:15 - chamber closing again? (Chamber-closing2). Current jumped to 0 for a second before the test, but the test ran smoothly.

5:20 - ready to test.

5:29 - t1-argon-9.7 running for 24 cycles (2 minutes). SCRATCH

5:30 - redo. t1-argon-9.7-2

5:30-5:42 - discussing test strategy with rocky

6:13 - changed strategy. Need to have delta T in checkerboard to get info we want.

6:15 t1-argon-9.7-3 - higher flux test. Null run, jtag fail

6:22 t1-argon-9.7-4

6:49 - t1-argon-9.7-6 with delta t in checker

7:22 test-cont continuous printing

7:48 - t1-argon-9.7-low-flux-newSW and redo both show a MBE that doesnt go away Redo2 is nothing

8:07 run6-argon-9.7 2 minute run. Transient MBE. 8:12 run6-argon-9.7-reset See if mbe persists. It persists.

8:23 figured out schedule

11:06 board2 Current draw seems to be different. During test 24mA on 3V3 (compared to 17mA before).

4:21 - returned. Jeff pretty much did board2 from 11-4.

4:21 - run66-xenon-58-1e7 45000 - 250 flux 70000- 2000 flux 100000- 3e4

4:30 - run67 16mA 3V3 and 52mA normal Limits raised to 500mA on both 1.5V dropped to 47mA then 22mA 3.3V raised to 25mA then down to 18mA 210mA 1.5V and 10mA on 3V3 3.2e6

4:36 - run68 same as 67 Dropped to 4mA and stayed there

4:40 - run69 same as 68 52-¿22-¿26 stayed up to 1e7

5:02 - run70 crypto 1e7 52-¿47-¿52-¿47-¿52-¿47-¿26

5:08 - run71 scratch

Vorago radtest 6/23 1:06 PM

Device 3

Board has 6mA on 3V3 which was different than other boards. Current on 1V5 is similar. HOWEVER this could be due to the I/O not being exercised like before.

Investigate this: Error: JTAG-DP STICKY ERROR Error: Failed to read memory at 0xaa4d549a Error: address + size wrapped (0xffffffff, 0x00000004)

New testing strategy. Focus only on RAM. Four passes - zeros, 1s, checker, anti-checker

1:17 run78 argon Invalid numbers

1:27 run79 argon Fixed scrub settings 10 for rom, 0 for ram. Current draw went up 2mA on 1V5

1:30 run80 argon Higher flux.

2:42 run93 boron Higher flux. Some issues on the tabview side of things

SKIPPED 94

3:04 run96 copper Flux started super low.

3:10 run97 copper NOTE: the code magically restarted here. After cycle 22 it restarted to 0 and printed everything out.

3:31 run102 krypton trial didnt output 23 cycles as before. Could be due to prints happening slower or becoming stuck

3:39 run103 krypton Encountered same issue as run97. After cycle 14, restarted back to 0. Run103-debug. Ran without beam to see if issue would happen again.

3:52 run104 xenon broke. SEFI? Current dropped to 25mA on 1V5. I gave it a soft reset and continued below Run104-cont Resume at 25000

3:58 run105 xenon (No timer, ran a little longer)

4:01 run106 xenon fault. Error: Debug regions are unpowered, an unexpected reset might have happened Error: JTAG-DP STICKY ERROR target halted due to undefined, current mode: Thread Gave it soft reset. Run106-cont Beam never stopped.

4:09 run 107 xenon Possible MBE??? Anti pattern error??? Cycle 1

4:12 run 108 xenon Higher flux Interesting run Run108-cont Error: Could not find MEM-AP to control the core After soft reset Current has been normal Good after hard reset (cont2)

4:18 run109 xenon MBE is always 4 x checkerboard errors Board hung. 34mA. jtag debugger did not complain (Cont) begun normally.

4:21 run110 xenon Max scrub rates Whoops. Forgot to make (-scrub) max scrub. Stuck in boot print loop? With scrub, current is 46mA. Hard reset required. MEM_AP error

4:25 run111 xenon Max scrub Doing really well, no MBE, then suddenly board froze up. Current same. Worked after soft reset. (-cont)

4:30 run112 xenon Max scrub, long duration, low flux

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[6] Kim, V.-K. and T. Chen. "On comparing functional fault coverage and defect coverage for memory testing". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 18.11 (1999), pp. 1676–1683.

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